

Data sheet acquired from Harris Semiconductor  
SCHS153C

## High-Speed CMOS Logic Quad 2-Input Multiplexers

September 1997 - Revised October 2003

### Features

- Common Select Inputs
- Separate Enable Inputs
- Buffered inputs and Outputs
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC157, 'HCT157, 'HC158, and 'HCT158 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Enable input ( $\bar{E}$ ) is active Low. When ( $\bar{E}$ ) is High, all of the outputs in the 158, the inverting type, ( $1\bar{Y}$ - $4\bar{Y}$ ) are forced High and in the 157, the non-inverting type, all of the outputs ( $1\bar{Y}$ - $4\bar{Y}$ ) are forced Low, regardless of all other input conditions.

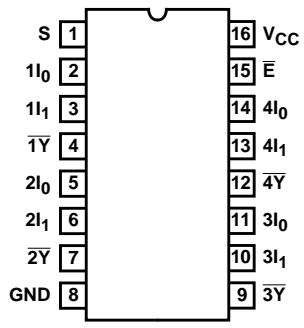
Moving data from two groups of registers to four common output buses is a common use of these devices. The state of the Select input determines the particular register from which the data comes. They can also be used as function generators.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC157F3A	-55 to 125	16 Ld CERDIP
CD54HCT157F3A	-55 to 125	16 Ld CERDIP
CD54HCT158F3A	-55 to 125	16 Ld CERDIP
CD74HC157E	-55 to 125	16 Ld PDIP
CD74HC157M	-55 to 125	16 Ld SOIC
CD74HC157MT	-55 to 125	16 Ld SOIC
CD74HC157M96	-55 to 125	16 Ld SOIC
CD74HCT157E	-55 to 125	16 Ld PDIP
CD74HCT157M	-55 to 125	16 Ld SOIC
CD74HCT157MT	-55 to 125	16 Ld SOIC
CD74HCT157M96	-55 to 125	16 Ld SOIC
CD74HCT158E	-55 to 125	16 Ld PDIP

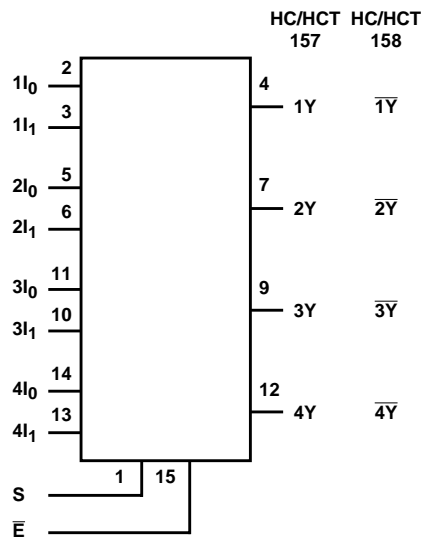
### Pinout

CD54HC157, CD54HCT157, CD54HC158, CD54HCT158 (CERDIP)  
 CD74HC157, CD74HCT157, CD74HC158 (PDIP, SOIC)  
 CD74HCT158 (PDIP)  
 TOP VIEW



NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

**Functional Diagram**



TRUTH TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT	
				157	158
$\bar{E}$	S	I0	I1	Y	$\bar{Y}$
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

**Absolute Maximum Ratings**

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 7V  
 DC Input Diode Current,  $I_{IK}$   
 For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
 For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  or  $I_{GND}$  .....  $\pm 50mA$

**Thermal Information**

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  ( $^{\circ}C/W$ )  
 E (PDIP) Package ..... 67  
 M (SOIC) Package ..... 73  
 Maximum Junction Temperature .....  $150^{\circ}C$   
 Maximum Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) .....  $300^{\circ}C$   
 (SOIC - Lead Tips Only)

**Operating Conditions**

Temperature Range ( $T_A$ ) .....  $-55^{\circ}C$  to  $125^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$   
 HC Types ..... 2V to 6V  
 HCT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I, V_O$  ..... 0V to  $V_{CC}$   
 Input Rise and Fall Time  
 2V ..... 1000ns (Max)  
 4.5V ..... 500ns (Max)  
 6V ..... 400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1. The package thermal impedance is calculated in accordance with JESD 51-7.

**DC Electrical Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$

## DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

2. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

INPUT	UNIT LOADS	
	HCT157	HCT158
I (All)	0.95	0.4
$\bar{E}$	0.6	0.6
S	3	2.8

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

Switching Specifications Input t<sub>p</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC/HCT157 TYPES</b>											
Propagation Delay (Figure 1) Data to Output	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	125	-	155	-	190	ns
			4.5	-	-	25	-	31	-	38	ns
HC157		C <sub>L</sub> = 15pF	5	-	10	-	-	-	-	-	ns
			HCT157	-	12	-	-	-	-	-	ns
HCT157		C <sub>L</sub> = 50pF	6	-	-	21	-	26	-	32	ns

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Enable to Output	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
HC157	$t_{PLH}, t_{PHL}$	$C_L = 15\text{pF}$	5	-	11	-	-	-	-	-	ns
HCT157				-	12	-	-	-	-	-	ns
Select to Output	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	6	-	-	23	-	29	-	35	ns
			2	-	-	145	-	180	-	220	ns
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	-	5	-	62	-	-	-	-	-	pF
				-	70	-	-	-	-	-	pF
<b>HC/HCT158 TYPES</b>											
Data to Output	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	140	-	175	-	210	ns
			4.5	-	-	28	-	35	-	42	ns
HC158	$t_{PLH}, t_{PHL}$	$C_L = 15\text{pF}$	5	-	11	-	-	-	-	-	ns
HCT 158				-	13	-	-	-	-	-	ns
Enable to Output	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	6	-	-	24	-	30	-	36	ns
			2	-	-	160	-	200	-	240	ns
Select to Output	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	32	-	40	-	48	ns
			5	-	13	-	-	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	5	-	13	-	-	-	-	-	ns
			6	-	-	27	-	34	-	41	ns
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	-	5	-	35	-	-	-	-	-	pF
				-	35	-	-	-	-	-	pF
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF

## NOTES:

- $C_{PD}$  is used to determine the dynamic power consumption, per multiplexer.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

**Test Circuits and Waveforms**

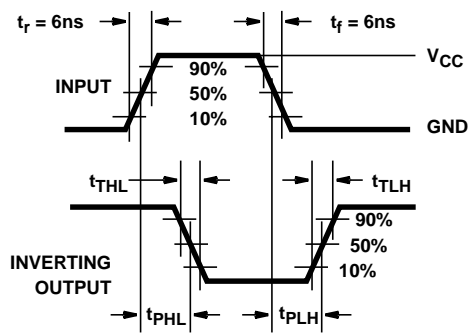


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

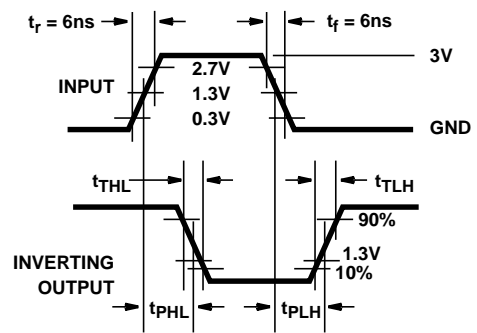


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

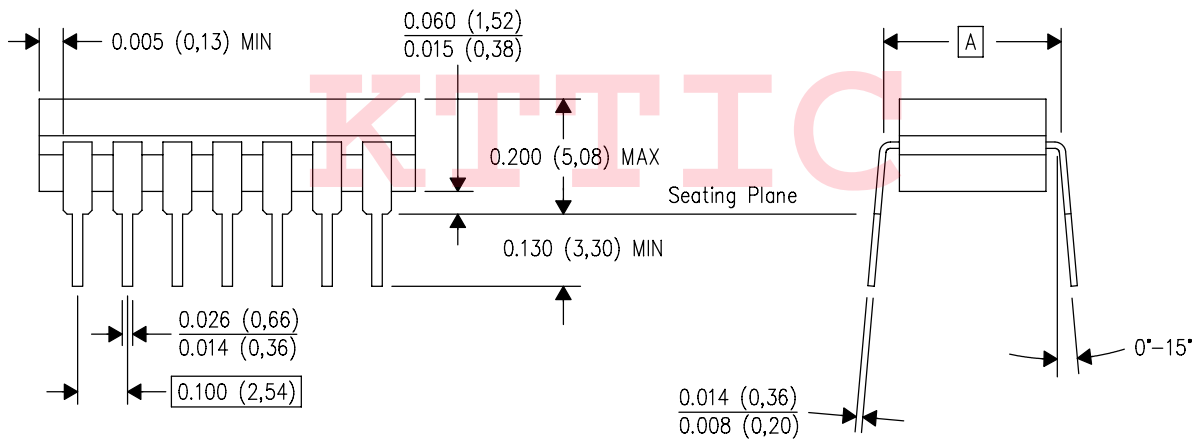
KTTIC

J (R-GDIP-T\*\*)  
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



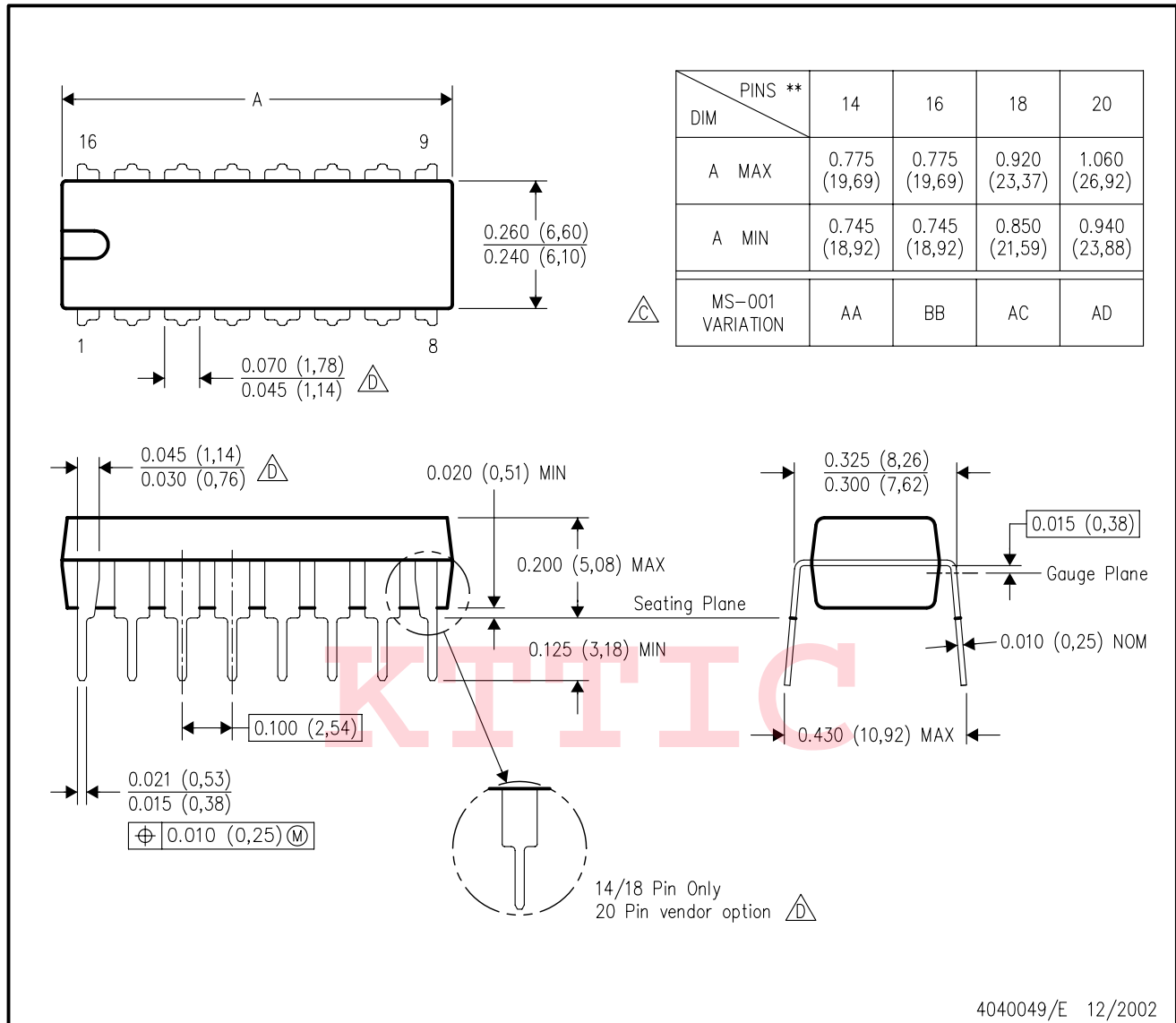
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



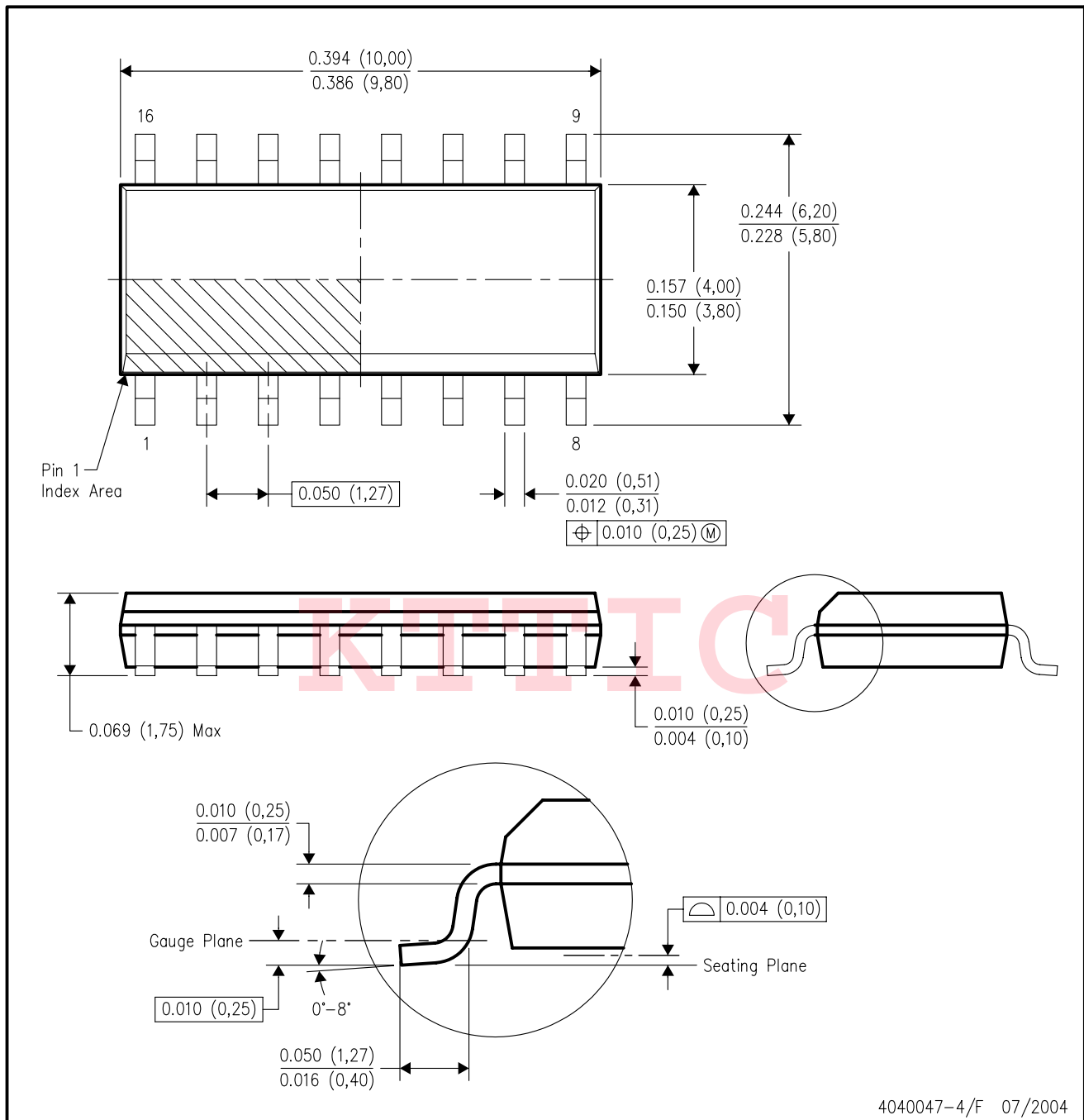
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

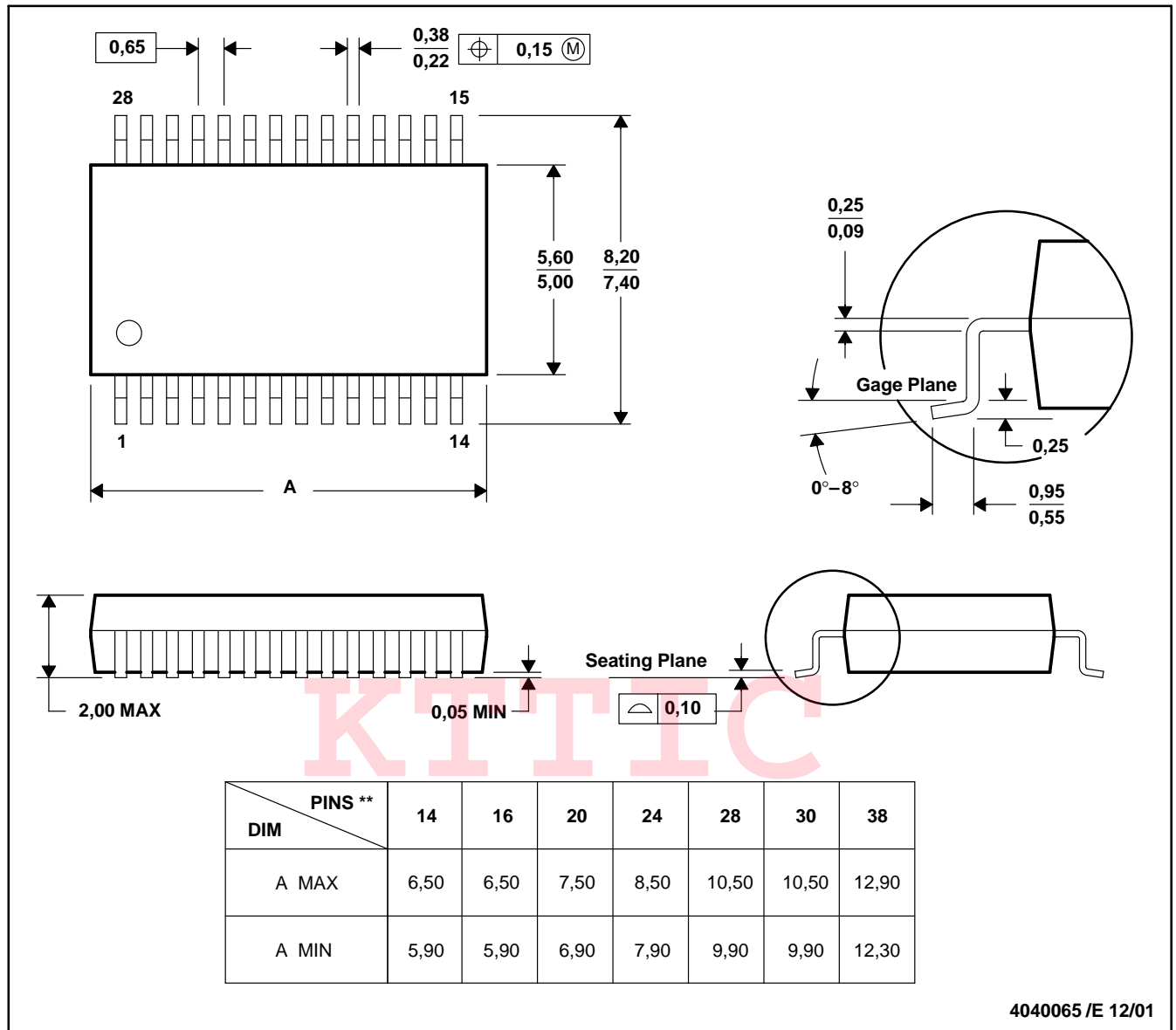


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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