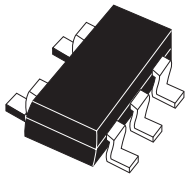
STWD100

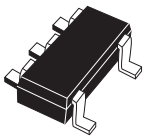
Watchdog timer circuit

Features

- Current consumption 13 µA typ.
- Available watchdog timeout periods are 3.4 ms, 6.3 ms, 102 ms and 1.6 s
- Chip-enable input
- Open drain or push-pull $\overline{\text{WDO}}$ output
- Operating temperature range: –40 to +125 °C
- Package SOT23-5, SC70-5 (SOT323-5)



SOT23-5 (WY)



SC70-5,
SOT323-5 (W8)

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1 Description

The STWD100 watchdog timer circuits are self-contained devices which prevent system failures that are caused by certain types of hardware errors (non-responding peripherals, bus contention, etc.) or software errors (bad code jump, code stuck in loop, etc.).

The STWD100 watchdog timer has an input, WDI, and an output, $\overline{WDO}$ (see *Figure 2*). The input is used to clear the internal watchdog timer periodically within the specified timeout period, t_{wd} (see *Section 3: Watchdog timing*). While the system is operating correctly, it periodically toggles the watchdog input, WDI. If the system fails, the watchdog timer is not reset, a system alert is generated and the watchdog output, $\overline{WDO}$, is asserted (see *Section 3: Watchdog timing*).

The STWD100 circuit also has an enable pin, $\overline{EN}$ (see *Figure 2*), which can enable or disable the watchdog functionality. The $\overline{EN}$ pin is connected to the internal pull-down resistor. The device is enabled if the $\overline{EN}$ pin is left floating.

Figure 1. SOT23-5 and SC70-5 (SOT323-5) package connections

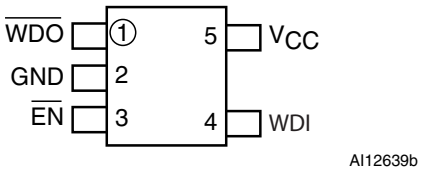
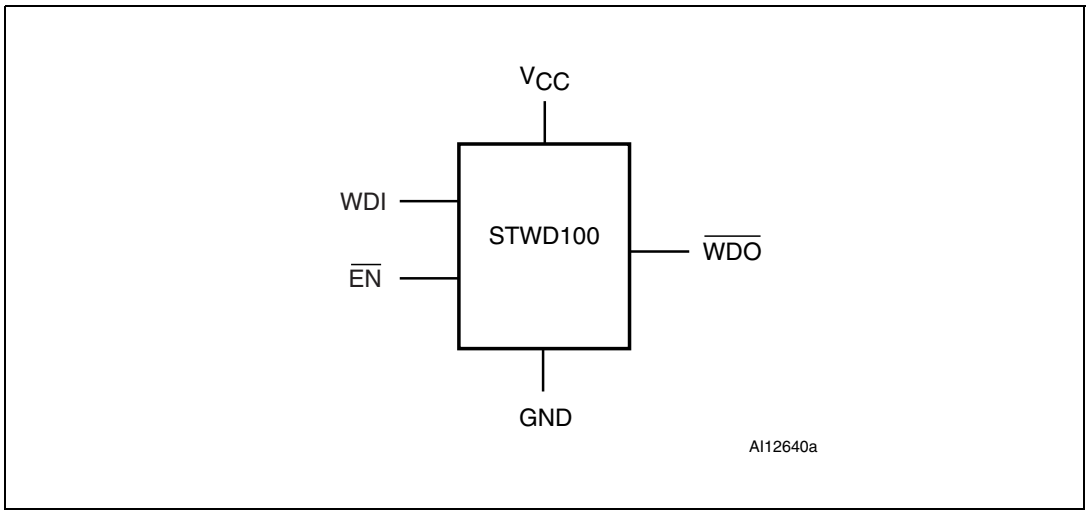


Table 1. SOT23-5 and SC70-5 (SOT323-5) pin description

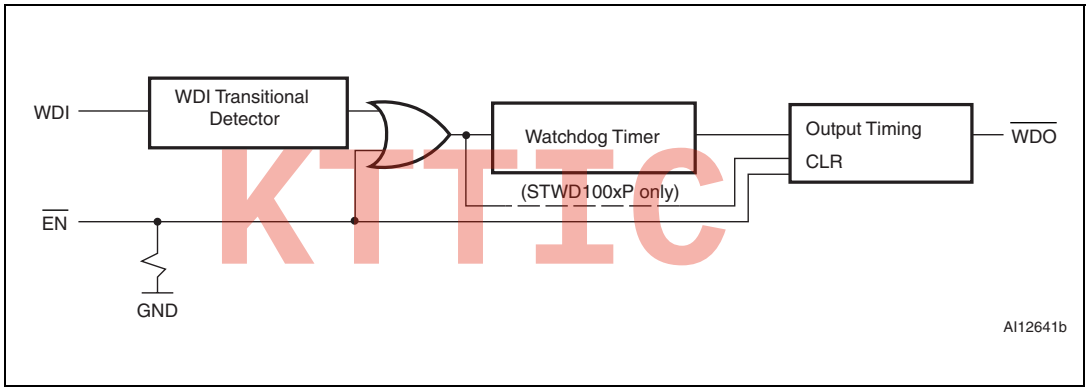
Pin number	Name	Description
1	$\overline{WDO}$	Watchdog output
2	GND	Ground
3	$\overline{EN}$	Enable pin
4	WDI	Watchdog Input
5	V_{CC}	Supply voltage

Figure 2. Logic diagram



Note: $\overline{WDO}$ output is available in open drain or push-pull configuration.

Figure 3. Block diagram



Note: Positive pulse on enable pin $\overline{EN}$ longer than 1 µs resets the watchdog timer.

2 Operation

The STWD100 device is used to detect an out-of-control MCU. The user has to ensure watchdog reset within the watchdog timeout period, otherwise the watchdog output is asserted and MCU is restarted. The STWD100 can be also enabled or disabled by the chip-enable pin.

2.1 Watchdog input (WDI)

The WDI input has to be toggled within the watchdog timeout period, t_{WD}, otherwise the watchdog output, $\overline{WDO}$, is asserted. The internal watchdog timer, which counts the t_{WD} period, is cleared either:

1. by a transition on watchdog output, $\overline{WDO}$ (see *Figure 8*) or
2. by a pulse on enable pin, $\overline{EN}$ (see *Figure 10*) or
3. by toggling WDI input (low-to-high on all versions and high-to-low on STWD100xW, STWD100xX and STWD100xY only).

The pulses on WDI input with a duration of at least 1 µs are detected and glitches shorter than 100 ns are ignored.

If WDI is permanently tied high or low and $\overline{EN}$ is tied low, the $\overline{WDO}$ toggles every 3.4 ms (t_{WD}) on STWD100xP and every t_{WD} and t_{PW} on STWD100xW, STWD100xX and STWD100xY (see *Figure 8*).

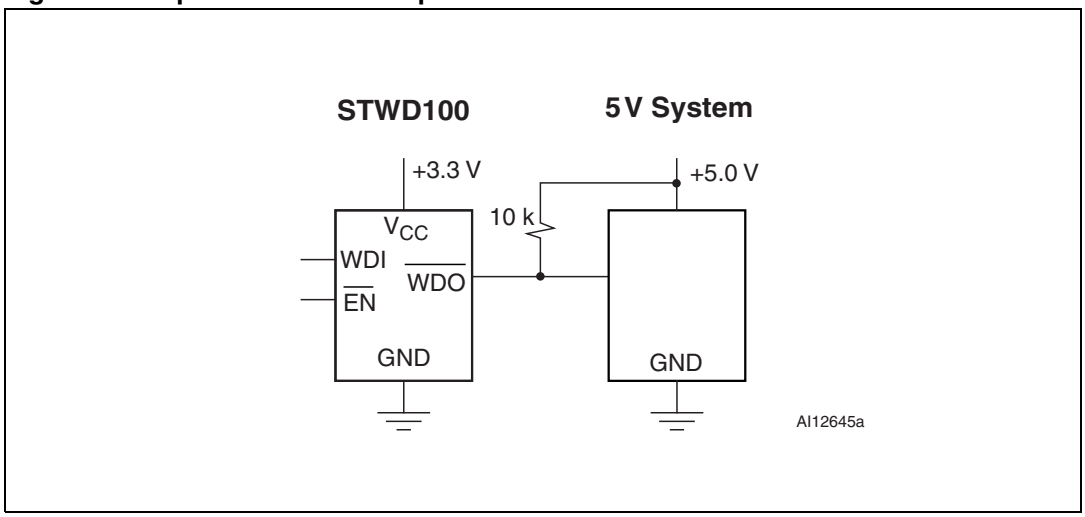
2.2 Watchdog output ($\overline{WDO}$)

When the V_{CC} exceeds the timer startup voltage V_{START} after power-up, the internal watchdog timer starts counting. If the timer is not cleared within the t_{WD}, the $\overline{WDO}$ will go low (see *Figure 6*).

After exceeding the t_{WD}, the $\overline{WDO}$ is asserted for t_{PW} on STWD100xW, STWD100xX and STWD100xY regardless of possible WDI transitions (see *Figure 9*). On STWD100xP $\overline{WDO}$ is asserted for a minimum of 10 µs and a maximum of t_{WD} after exceeding the t_{WD} period (see *Figure 8* and *Figure 9*).

The STWD100 has an active-low open drain or push-pull output. An external pull-up resistor connected to any supply voltage up to 6 V is required in case of open drain $\overline{WDO}$ output (see *Figure 4*). Select a resistor value large enough to register a logic low, and small enough to register a logic high while supplying all input current and leakage paths connected to the reset output line. A 10 kΩ pull-up resistor is sufficient in most applications.

Figure 4. Open drain $\overline{WDO}$ output connection



2.3 Chip-enable input ($\overline{EN}$)

All states mentioned in *Section 2.1: Watchdog input (WDI)* and *Section 2.2: Watchdog output (WDO)* are valid under the condition that $\overline{EN}$ is in logical low state.

The behavior of $\overline{EN}$ is common to all versions (i.e. STWD100xP, STWD100xW, STWD100xX and STWD100xY).

If the $\overline{EN}$ goes high after power-up in less than t_{WD} from the moment that V_{CC} exceeds the timer startup voltage, V_{START}, the $\overline{WDO}$ will stay high for the same time period as $\overline{EN}$, plus t_{WD} (see *Figure 10*).

If the $\overline{EN}$ goes high anytime during normal operation, the $\overline{WDO}$ will go high as well, but the minimum possible $\overline{WDO}$ pulse width is 10 µs (see *Figure 10*).

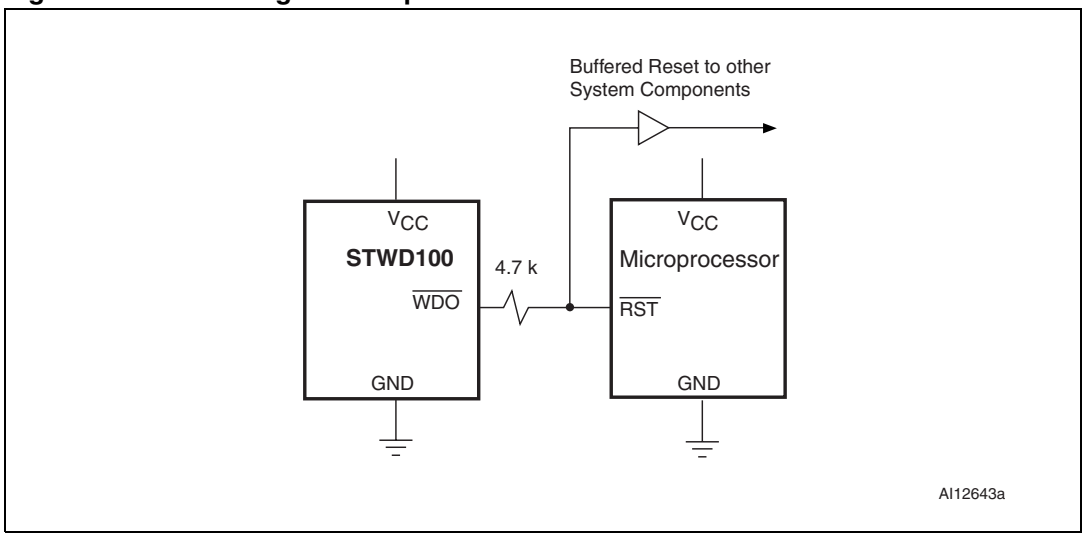
The pulses on the $\overline{EN}$ pin with a duration of at least 1 µs are detected and glitches shorter than 100 ns are ignored.

2.4 Applications information

2.4.1 Interfacing to microprocessors with bidirectional reset pins

Microprocessors with bidirectional reset pins can contend with the STWD100 watchdog output, $\overline{WDO}$. For example, if the $\overline{WDO}$ output is driven high and the micro wants to pull it low, signal contention will result. To prevent this from occurring, connect a 4.7 kΩ resistor between the $\overline{WDO}$ output and the micro's reset I/O as in *Figure 5*.

Figure 5. Interfacing to microprocessors with bidirectional reset I/O



3 Watchdog timing

Figure 6. Power-up

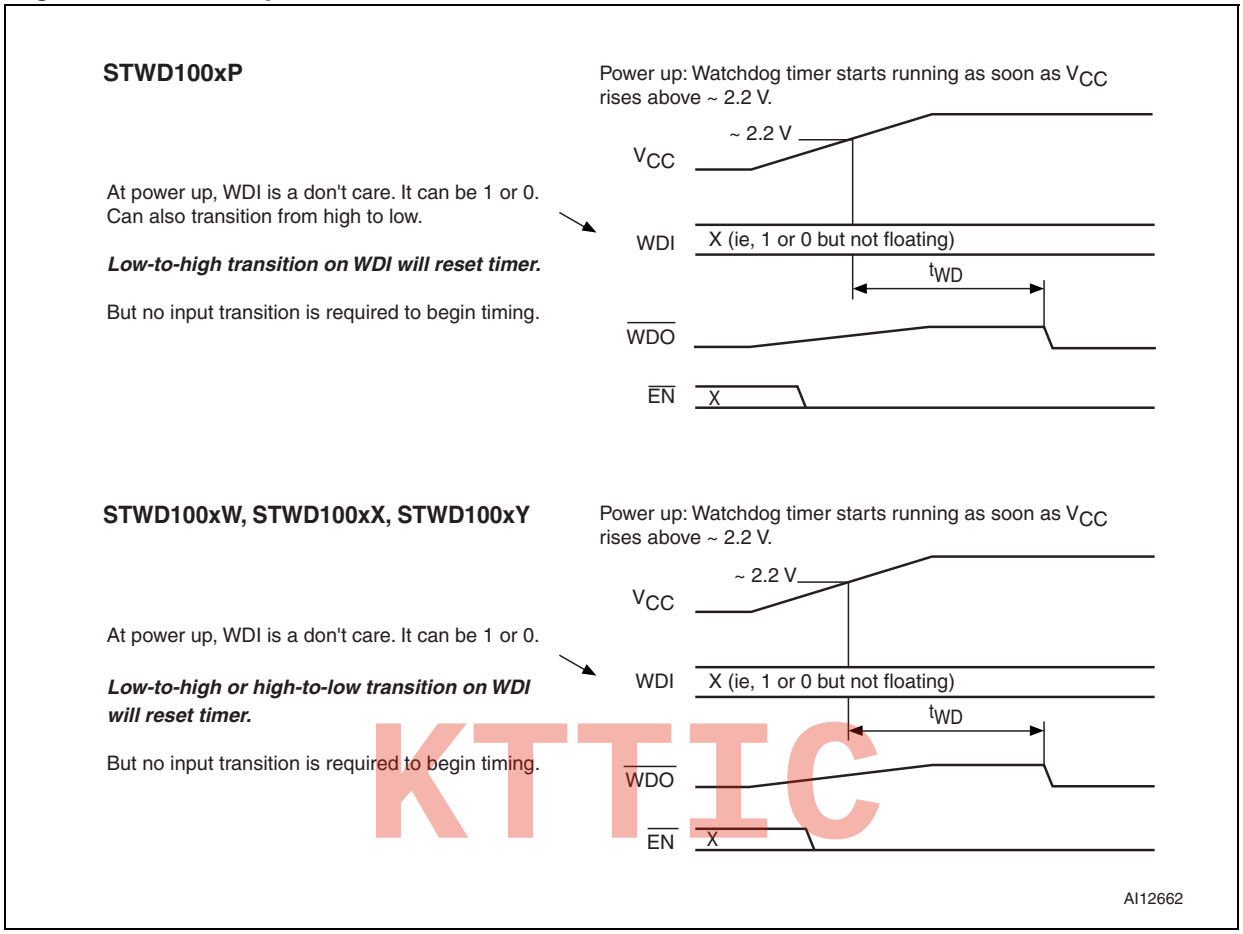


Figure 7. Normal triggering

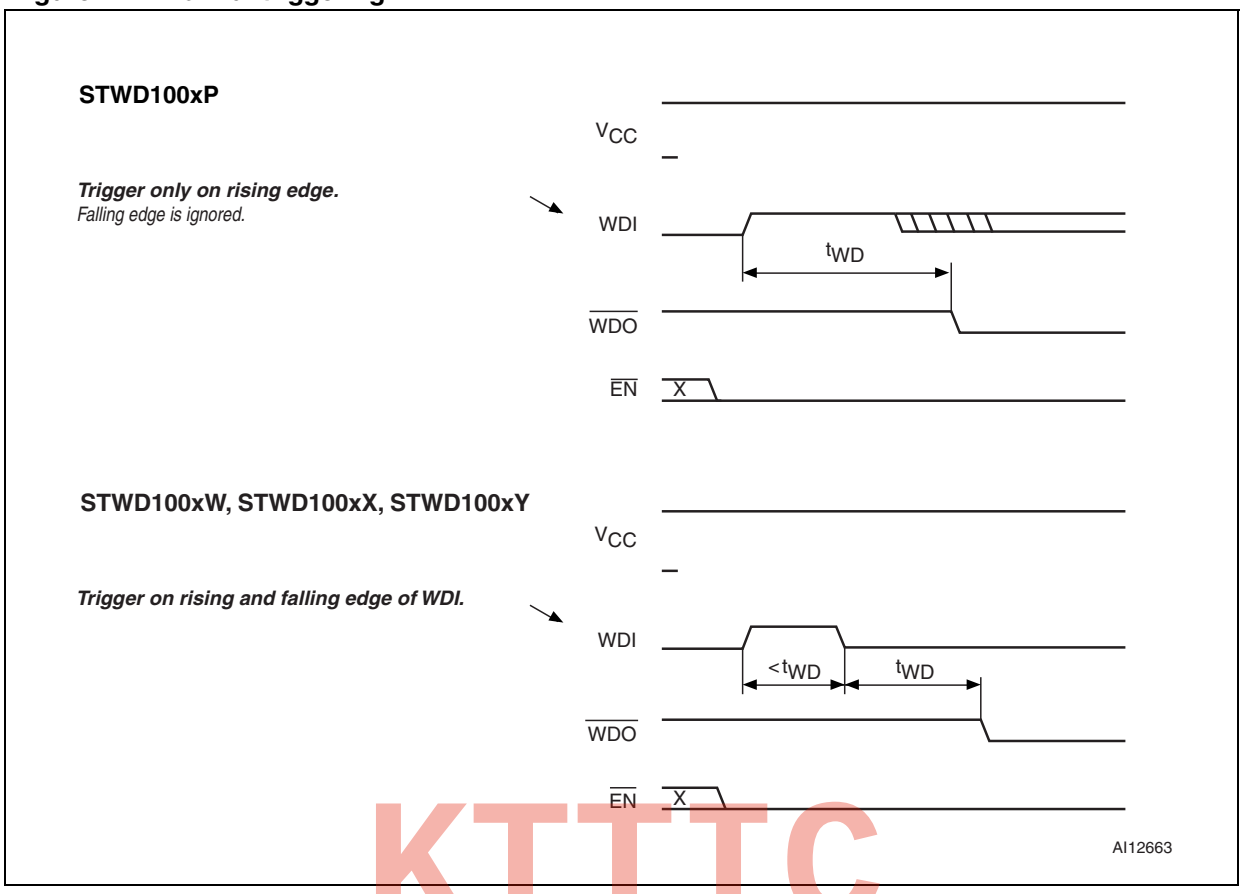


Figure 8. Timeout without re-trigger

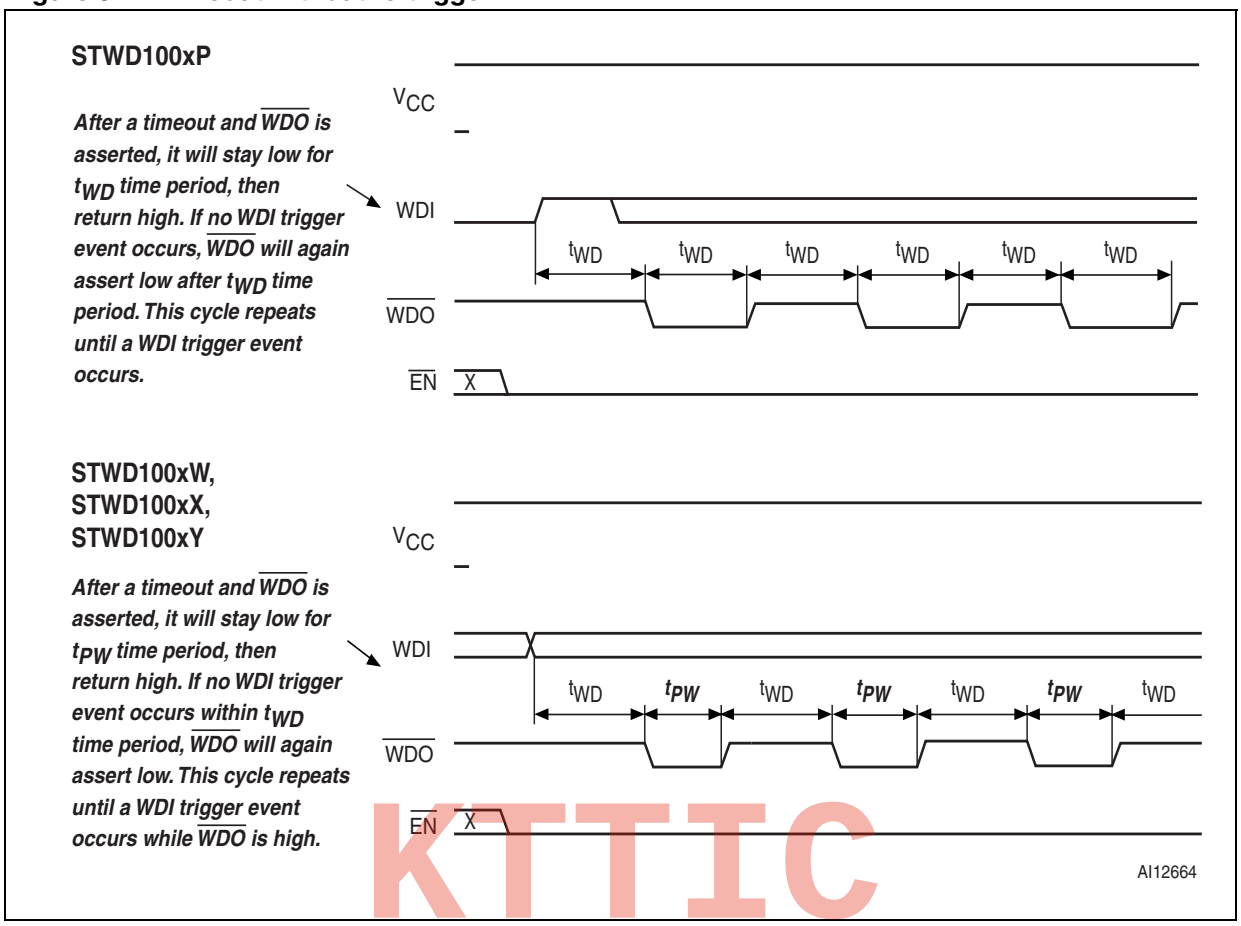


Figure 9. Trigger after timeout

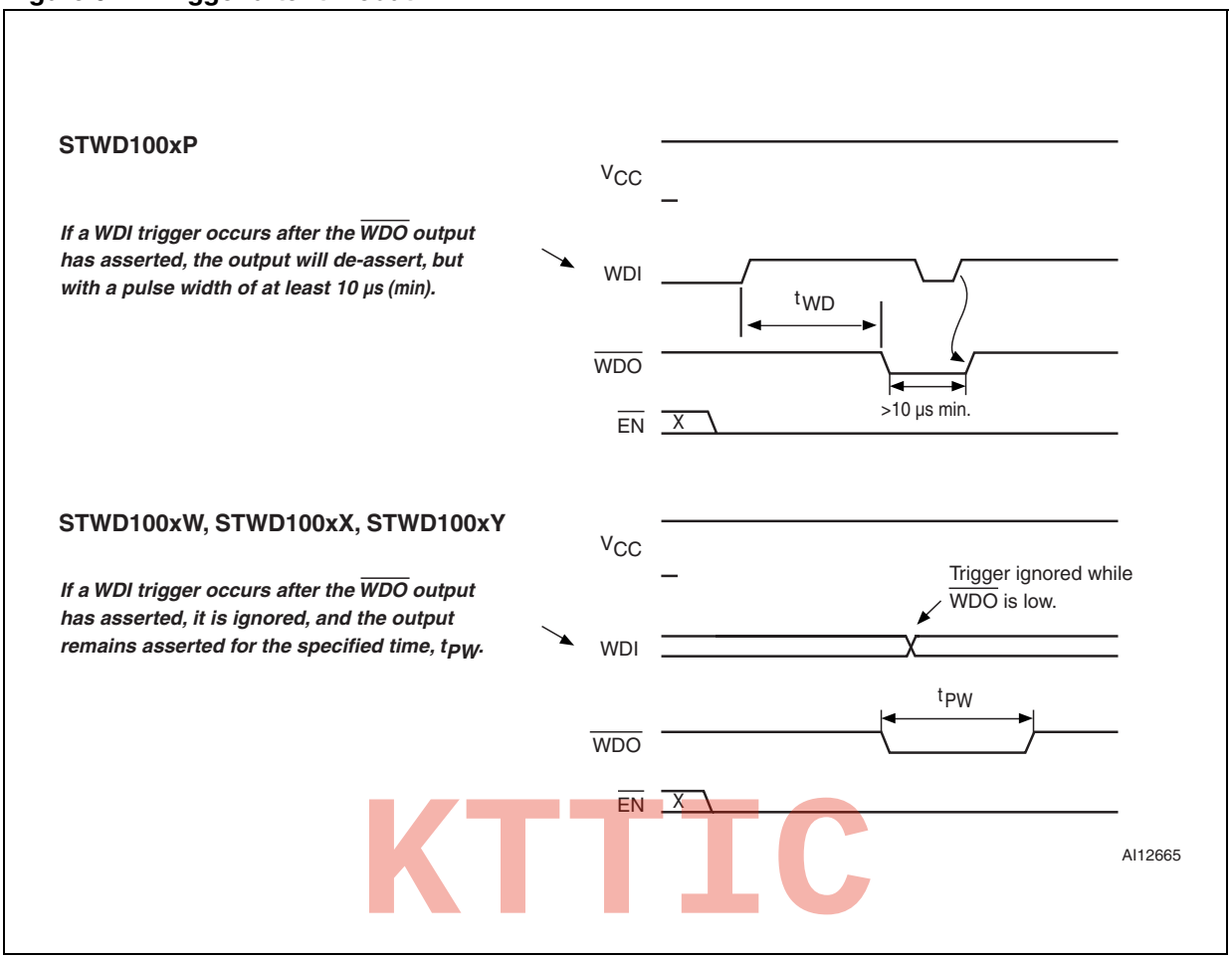
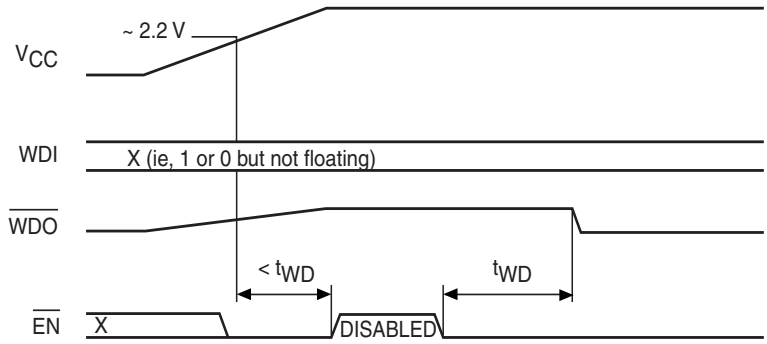


Figure 10. Enable pin, $\overline{EN}$, triggering

STWD100xx

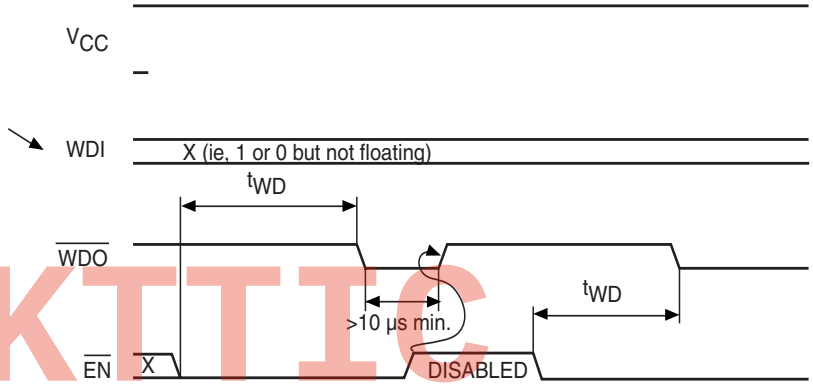
Whenever $\overline{EN}$ is high, all timing is reset, and the part is disabled.

Timing commences from 0 when $\overline{EN}$ goes low.



STWD100xx

If $\overline{EN}$ goes high while $\overline{WDO}$ is asserted, $\overline{WDO}$ will de-assert but only after the nominal minimum pulse width of 10 µs has elapsed.



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4 Maximum ratings

Stressing the device above the rating listed in *Table 2* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off)	–55 to 150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltage	–0.3 to V_{CC} +0.3	V
V_{CC}	Supply voltage	–0.3 to 7.0	V
I_O	Output current	20	mA
PD	Power dissipation	320	mW

1. Reflow at peak temperature of 260 °C (total thermal budget not to exceed 245 °C for greater than 30 seconds).

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 3*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 3. Operating and AC measurement conditions

Parameter	Value	Unit
V_{CC} supply voltage	2.7 to 5.5	V
Ambient operating temperature (T_A)	–40 to 125	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V_{CC}	V
Input and output timing ref. voltages	0.3 to 0.7 V_{CC}	V

Table 4. DC and AC characteristics

Sym	Description	Test condition(1)	Min	Typ	Max	Unit
V_{CC}	Operating voltage		2.7	5	5.5	V
I_{CC}	V_{CC} supply current			13	26	µA
I_{LO}	Open drain output leakage current	from output to the GND or V_{CC}	–1		+1	µA
	Input leakage current (WDI)		–1		+1	µA
V_{IH}	Input high voltage (WDI, $\overline{EN}$)		0.7 V_{CC}			V
V_{IL}	Input low voltage (WDI, $\overline{EN}$)				0.3 V_{CC}	V
V_{OL}	Output low voltage ($\overline{WDO}$)	$V_{CC} \geq 2.7$ V, $I_{SINK} = 1.2$ mA			0.3	V
		$V_{CC} \geq 4.5$ V, $I_{SINK} = 3.2$ mA			0.4	V
V_{OH}	Output high voltage ($\overline{WDO}$) (push-pull only)	$V_{CC} \geq 2.7$ V, $I_{SOURCE} = 500$ µA	0.8 V_{CC}			V
		$V_{CC} \geq 4.5$ V, $I_{SOURCE} = 800$ µA	0.8 V_{CC}			V
Enable pin ($\overline{EN}$)						
	$\overline{EN}$ input pulse width		1			µs
	$\overline{EN}$ glitch rejection			100		ns
	$\overline{EN}$-to-$\overline{WDO}$ delay(2)			200		ns
	$\overline{EN}$ pull-down resistance		32	63	100	kΩ
Watchdog Timer						
V_{START}	Timer startup voltage		1.9	2.2	2.7	V
t_{WD}	Watchdog timeout period	STWD100xP	2.3	3.4	4.6	ms
		STWD100xW	4.3	6.3	8.6	ms
		STWD100xX	71	102	142	ms
		STWD100xY	1.12	1.6	2.24	s
t_{PW}	Watchdog active time		140	210	280	ms
	WDI-to-$\overline{WDO}$ delay(3)			150		ns
	WDI pulse width		1			µs
	WDI glitch rejection			100		ns

1. Valid for ambient operating temperature: $T_A = –40$ to 125 °C; $V_{CC} = 2.7$ V to 5.5 V except where noted.
2. $\overline{WDO}$ will assert for minimum of 10 µs even if $\overline{EN}$ transitions high.
3. $\overline{WDO}$ will assert for minimum of 10 µs regardless of transition on WDI (valid for STWD100xP only).

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 11. SOT23-5 - 5-lead small outline transistor package mechanical drawing

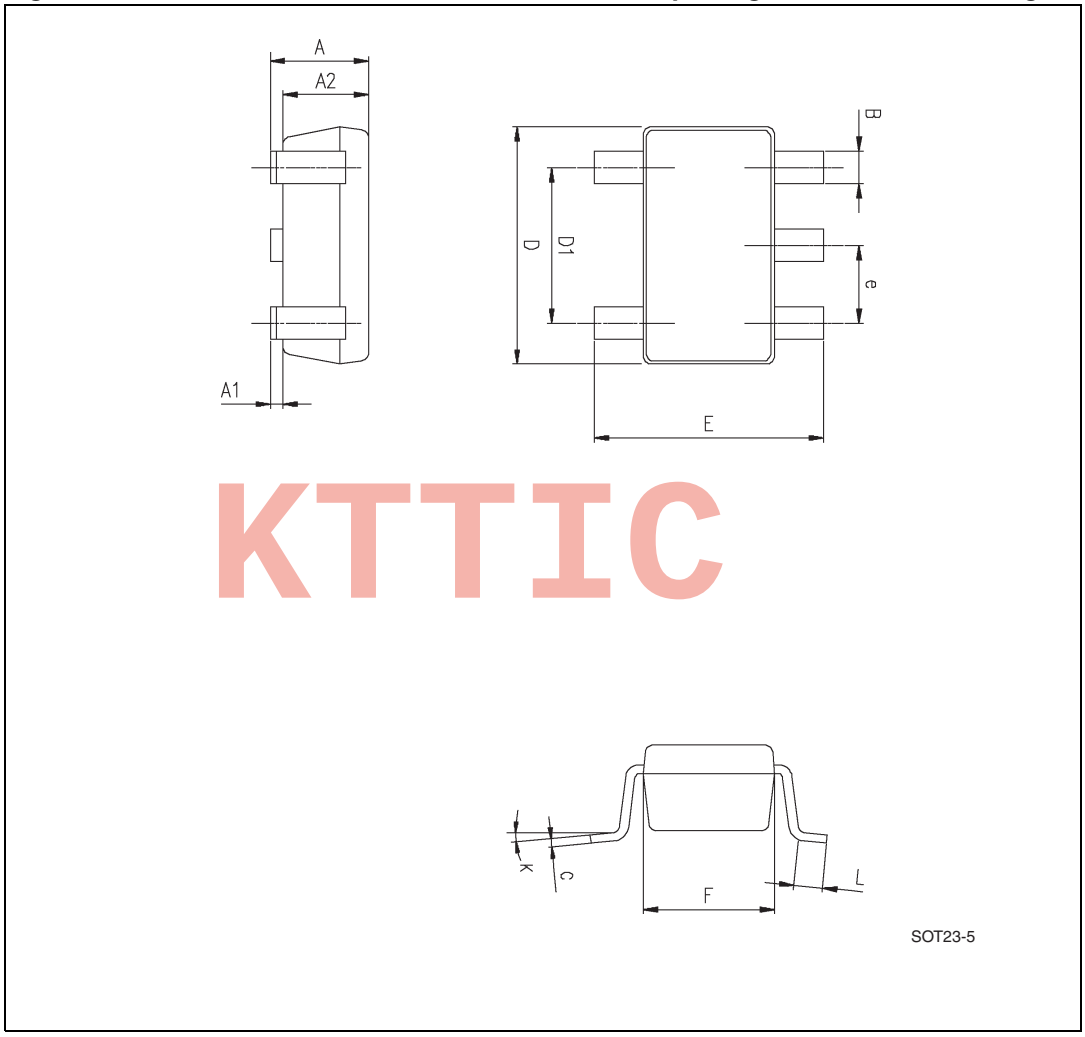

Table 5. SOT23-5 - 5-lead small outline transistor package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	1.20	0.90	1.45	0.047	0.035	0.057
A1			0.15			0.006
A2	1.05	0.90	1.30	0.041	0.035	0.051
B	0.40	0.35	0.50	0.016	0.014	0.020
C	0.15	0.09	0.20	0.006	0.004	0.008
D	2.90	2.80	3.00	0.114	0.110	0.118
D1	1.90			0.075		
E	2.80	2.60	3.00	0.110	0.102	0.118
e	0.95			0.037		
F	1.60	1.50	1.75	0.063	0.059	0.069
K		0°	10°		0°	10°
L	0.35	0.10	0.60	0.014	0.004	0.024

Figure 12. SC70 (SOT323-5) - 5-lead small outline transistor package outline

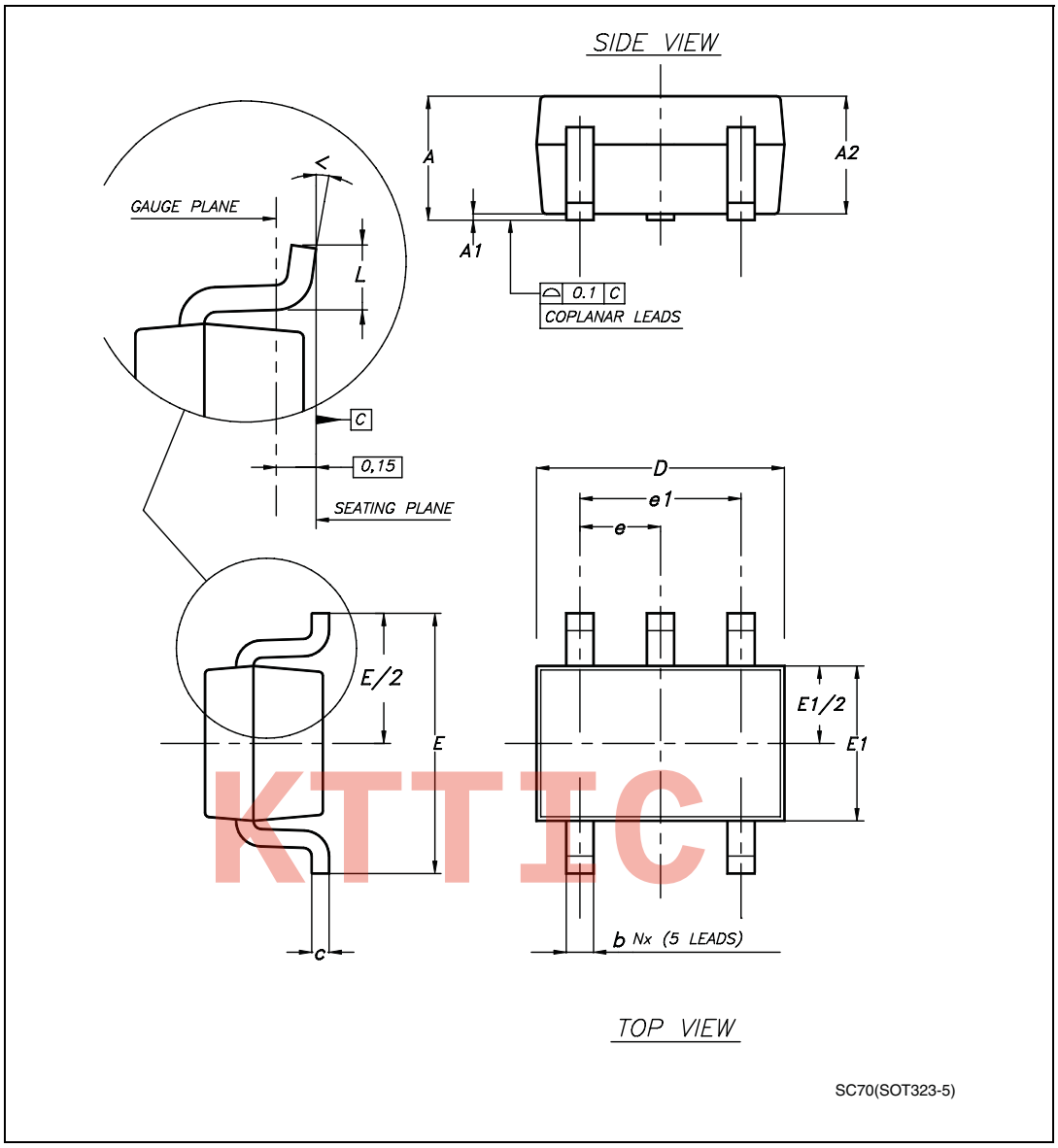

Table 6. SC70 (SOT323-5) – 5-lead small outline transistor package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		0.80	1.10		0.031	0.043
A1		0.00	0.10		0.000	0.004
A2	0.90	0.80	1.00	0.035	0.031	0.039
b		0.15	0.30		0.006	0.012
c		0.10	0.22		0.004	0.009
D	2.00	1.80	2.20	0.079	0.071	0.087
E	2.10	1.80	2.40	0.083	0.071	0.094
E1	1.25	1.15	1.35	0.049	0.045	0.053
e	0.65			0.026		
e1	1.30			0.051		
L	0.36	0.26	0.46	0.014	0.010	0.018
<	–	0°	8°	–	0°	8°
N	5			5		

7 Part numbering

Table 7. Ordering information scheme

Example: STWD100 N P WY 3 F

Device type

STWD100

Output type

N: Open drain (active low)

P: Push-pull (active low)

Device version

P: t_{WD} = 3.4 ms, t_{PW} = t_{WD} = 3.4 ms

W: t_{WD} = 6.3 ms, t_{PW} = 210 ms

X: t_{WD} = 102 ms, t_{PW} = 210 ms

Y: t_{WD} = 1.6 s, t_{PW} = 210 ms

Package

WY: SOT23-5

W8: SC70-5 (SOT323-5)

Temperature range

3: –40 to +125 °C

Shipping method

E: ECOPACK® package, tubes

F: ECOPACK® package, tape & reel

Note: Contact local ST sales office for availability of device versions other than STWD100NPWY3F.

8 Package marking information

Table 8. Device versions with marking descriptions

Part number(1)	Watchdog timing period		Output configuration	Topside marking	Bottomside marking(2)
	t_{wd}	t_{pw}			
STWD100NPxxxx	3.4 ms	3.4 ms	open drain	**WNP**	**PYWW**
STWD100NWxxxx	6.3 ms	210 ms	open drain	WNW	PYWW
STWD100NXxxxx	102 ms	210 ms	open drain	WNX	PYWW
STWD100NYxxxx	1.6 s	210 ms	open drain	WNY	PYWW
STWD100PWxxxx	6.3 ms	210 ms	push-pull	WPW	PYWW
STWD100PXxxxx	102 ms	210 ms	push-pull	WPX	PYWW
STWD100PYxxxx	1.6 s	210 ms	push-pull	WPY	PYWW

1. Contact local ST sales office for availability of device versions other than STWD100NPWY3F.
2. Description: P = assembly plant code, Y = assembly year (0 to 9), WW = assembly work week ((01 to 52).

9 Revision history

Table 9. Document revision history

Date	Revision	Changes
08-Nov-2007	1	Initial release.
23-Jan-2008	2	Updated cover page and *Table 4*; document status upgraded to full datasheet.
28-Jan-2008	3	Updated cover page.
17-Mar-2008	4	Updated cover page, *Figure 4*, *7*, *9*, and *Table 4*, *8*.
31-Jul-2008	5	Updated *Features* on cover page and *Table 4*.

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