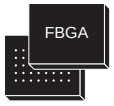
NAND256-M
NAND512-M, NAND01G-M

256/512Mb/1Gb (x8/x16, 1.8/3V, 528 Byte Page) NAND Flash Memories + 256/512Mb (x16/x32, 1.8V) LPSDRAM, MCP

Features

- Multi-Chip Packages
  - 1 die of 256 Mb, 512 Mb (x8/ x16) NAND Flash + 1 die of 256 Mb (x16) SDR LPSDRAM
  - 1 die of 256 Mb, 512 Mb (x8/ x16) NAND Flash + 2 dice of 256 Mb (x16) SDR LPSDRAMs
  - 1 die of 256 Mb, 512 Mb (x8/ x16) NAND Flash +1 die of 256 Mb (x16) DDR LPSDRAM
  - 1 die of 512 Mb (x16) NAND Flash + 1 die of 256 Mb or 512 Mb (x16) DDR LPSDRAM
- Supply voltages
  - V_{DDF} = 1.7V to 1.95V or 2.5V to 3.6V
  - V_{DDD} = V_{DDQD} = 1.7V to 1.9V
- Electronic Signature
- ECOPACK® packages
- Temperature range
  - -30 to 85°C



TFBGA107 10.5 x 13 x 1.2mm

TFBGA149 10 x 13.5 x 1.2mm

LFBGA137 10.5 x 13 x 1.4mm

TFBGA137 10.5 x 13 x 1.2 mm(1)

(1) Preliminary specifications.

Flash Memory

- NAND Interface
  - x8 or x16 bus width
  - Multiplexed Address/ Data
- Page size
  - x8 device: (512 + 16 spare) Bytes
  - x16 device: (256 + 8 spare) Words
- Block size
  - x8 device: (16K + 512 spare) Bytes
  - x16 device: (8K + 256 spare) Words
- Page Read/Program
  - Random access: 15µs (max)
  - Sequential access: 50ns (min)
  - Page program time: 200µs (typ)
- Copy Back Program mode
  - Fast page copy without external buffering
- Fast Block Erase
  - Block erase time: 2ms (typ)
- Status Register
- Data integrity
  - 100,000 Program/Erase cycles
  - 10 years Data Retention

LPSDRAM

- Interface: x16 or x 32 bus width
- Deep Power Down mode
- 1.8v LVCMOS interface
- Quad internal Banks controlled by BA0 and BA1
- Automatic and controlled Precharge
- Auto Refresh and Self Refresh
  - 8,192 Refresh cycles/64ms
  - Programmable Partial Array Self Refresh
  - Auto Temperature Compensated Self Refresh
- Wrap sequence: sequential/interleave
- Burst Termination by Burst Stop command and Precharge command

Table 1. Product List

Reference	Part Number	NAND Product	LPSDRAM Product	Package
NAND256-M	NAND256R3M0	256 Mbit (x8), 1.8V	256 Mbit SDR, (x16), 1.8V, 104MHz	TFBGA107
	NAND256R4M3	256Mbit (x16) 1.8V	256 Mbit DDR (x16) 1.8V, 133MHz	TFBGA149
	NAND256W3M4	256Mbit (x16) 3V	256 Mbit SDR (x16), 1.8V, 104MHz	TFBGA149
NAND512-M	NAND512R3M0	512 Mbit (x8), 1.8V	256 Mbit SDR (x16), 1.8V, 104MHz	TFBGA107
	NAND512R4M3		256 Mbit DDR (x16) 1.8V, 133MHz	TFBGA149
	NAND512R4M5		512 Mbit DDR (x16) 1.8V, 133MHz	TFBGA149
	NAND512W3M2	512Mbit (x8) 3V	512Mbit SDR (2x16) (2x256Mbit SDR x16) 1.8V,104Mhz	LFBGA 137
NAND01G-M	NAND01GW3M2	2 x 512Mbit NAND (x8) 3V	512 Mbit SDR (2x16) (2 x 256Mbit SDR x16) 1.8V, 104MHz	LFBGA137
		1 Gbit NAND (x8) 3V	512Mbit SDR (x32) 1.8V, 133MHz	TFBGA137

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1 Summary description

The NAND256-M, NAND512-M and NAND01G-M are Multi-Chip Packages which combine up to 512 Mbit LPSDRAM with a 256 Mbit, 512 Mbit or 1 Gbit NAND Flash memory. This combination of LPSDRAM and NAND Flash can result in up to 1 Gbit of memory.

The NAND Flash memory and LPSDRAM components have separate power supplies and grounds. They also have separate control, address and input/output signals, which allows simultaneous access to both devices at any moment.

They are distinguished by two chip enable inputs: $\overline{E}_F$ for the NAND Flash memory and $\overline{E}_D$ for the LPSDRAM. See *Figure 1: Logic Diagram: NAND Flash & 1 x SDR LPSDRAM* and *Table 2: Signal Names: NAND Flash & 1 x SDR LPSDRAM* for an overview of the signals attached to each component.

The NAND256-M, NAND512-M and NAND01G-M are available with a 1.8 or 3V voltage supply. See *Table 1: Product List* for a complete list of the products available.

The devices are offered in the following Multi-Chip packages:

- TFBGA107 (10.5 x 13 x 1.2mm)
- LFBGA137 (10.5 x 13 x 1.4mm)
- TFBGA149 (10 x 13.5 x 1.2mm)
- TFBGA137 (10.5 x 13 x 1.2mm)

In order to meet environmental requirements, ST offers the NAND256-M, NAND512-M and NAND01G-M devices in ECOPACK® package. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

The memories are supplied with all the NAND Flash memory bits erased (set to '1').

This datasheet should be read in conjunction with the NAND Flash and LPSDRAM datasheets.

NAND Flash Component

The NAND256-M, NAND512-M and NAND01G-M devices contain a 1.8V, 256 Mbit or 512 Mbit, x8 528 Byte Page or x16 264 Word Page, NAND Flash memory with the Chip Enable Don't Care option.
For detailed information on how to use the devices, see the NANDxxx-A and NAND01GWxA2B-KGD datasheets.

LPSDRAM Component

The NAND256-M and NAND512-M devices contain either:

- one M65KA256AL: 256Mbit (x16) Single Data Rate (SDR) LPSDRAM
- two M65KA256AL: 256Mbit (x16) Single Data Rate (SDR) LPSDRAMs (SDR_0 and SDR_1)
- one M65KG256AF: 256Mbit (x16) Double Data Rate (DDR) LPSDRAM
- one M65KG512AB: 512Mbit (x16) Double Data Rate (DDR) LPSDRAM
- one M65KC512AB: 512Mbit (x32) Single Data Rate (SDR) LPSDRAM

Refer to *Table 1: Product List*, for a description of the memories contained in the NAND256-M, NAND256-M and NAND01G-M devices.

For detailed information on how to use the SDR LPSDRAM devices, refer to the M65KA256AL and M65KC512AB datasheets which are available from your local STMicroelectronics distributor.

For detailed information on how to use the DDR LPSDRAM device, refer to the M65KG256AB datasheet which is available from your local STMicroelectronics distributor.

Figure 1. Logic Diagram: NAND Flash & 1 x SDR LPSDRAM

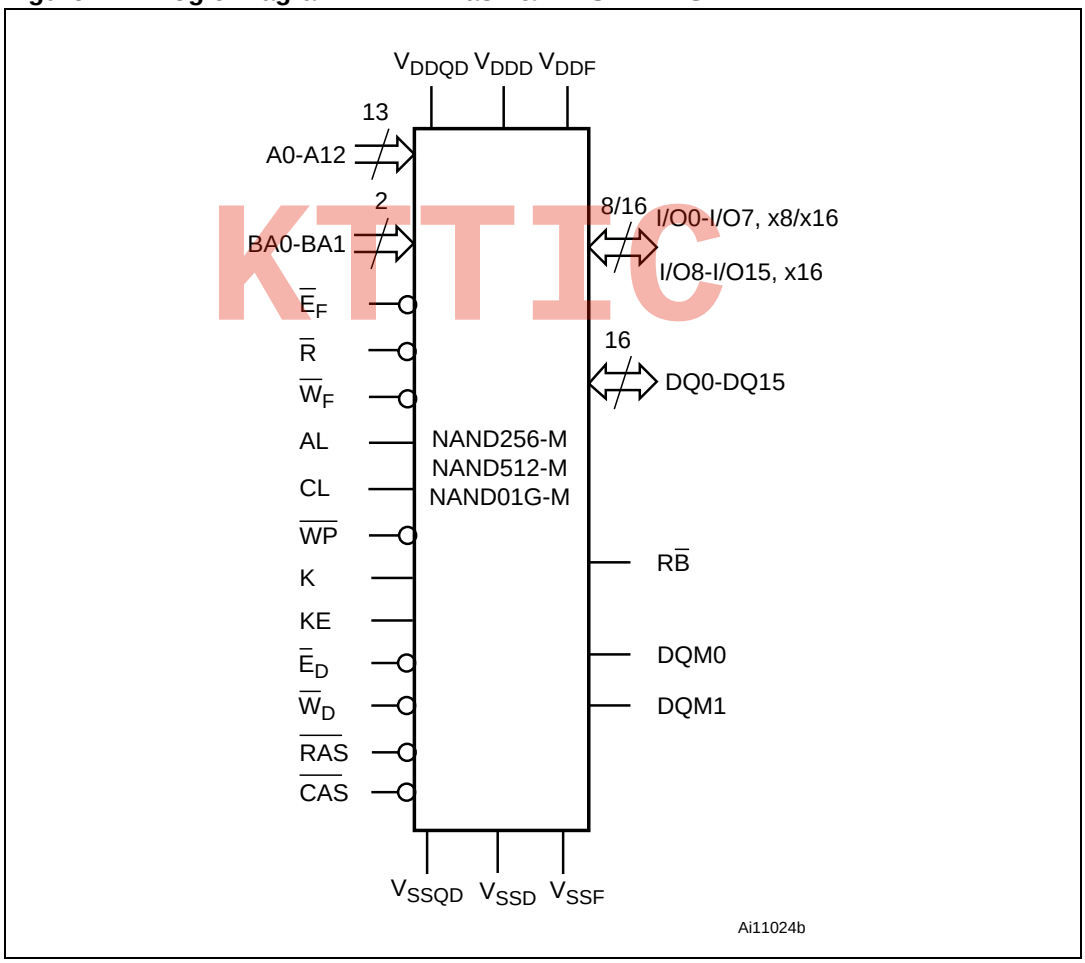


Table 2. Signal Names: NAND Flash & 1 x SDR LPSDRAM

NAND Flash	
I/O0-I/O7	Data Inputs/Outputs for x8 devices
I/O8-I/O15	Data Inputs/Outputs for x16 devices
AL	Address Latch Enable
CL	Command Latch Enable
$\overline{E}_F$	Chip Enable
R	Read Enable
$R\overline{B}$	Ready/Busy (open-drain output)
$\overline{W}_F$	Write Enable
$\overline{WP}$	Write Protect
V_{DDF}	Supply Voltage
V_{SSF}	Ground
SDR LPSDRAM	
A0-A12	Row Address: RA0-RA11 Column Address: CA0-CA8 Auto-precharge flag: A10
BA0-BA1	Bank Address
DQ0-DQ15	Data Inputs/Outputs
K	Clock Input
KE	Clock Enable Input
$\overline{E}_D$	Chip Select inputs
$\overline{W}_D$	Write Enable Input
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
DQM0	Upper DQ Mask Enable Output
DQM1	Lower DQ Mask Enable Output
V_{DDD}	Supply Voltage
V_{DDQD}	Input/Output Supply Voltage
V_{SSD}	Ground
V_{SSQD}	Input/Output Ground
NC	Not Connected Internally

Figure 2. Logic Diagram: NAND Flash & 2 x SDR LPSDRAMs

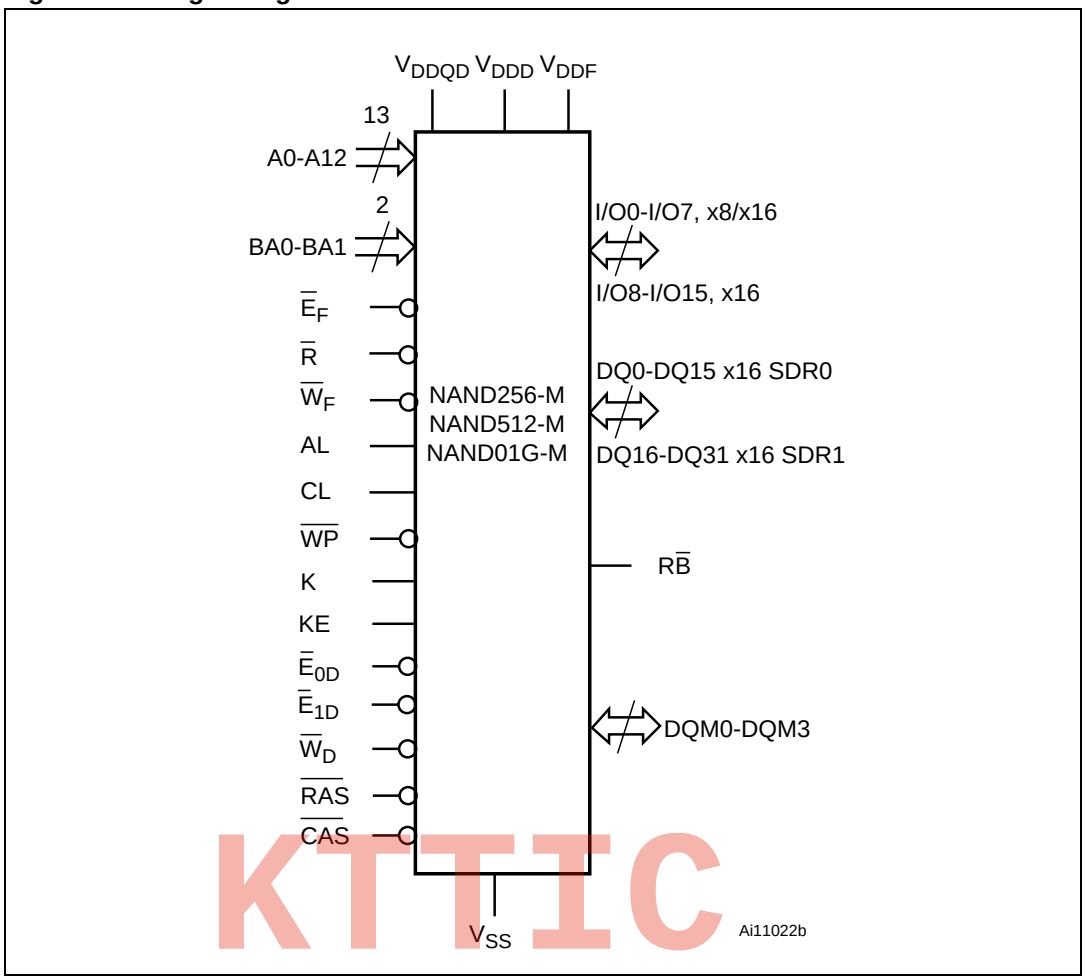


Table 3. Signal Names: NAND Flash & 2 x SDR LPSDRAMs

NAND Flash	
I/O0-I/O7	Data Inputs/Outputs
AL	Address Latch Enable
CL	Command Latch Enable
$\overline{E}_F$	Chip Enable
R	Read Enable
$R\overline{B}$	Ready/Busy (open-drain output)
$\overline{W}_F$	Write Enable
$\overline{WP}$	Write Protect
V_{DDF}	Supply Voltage
V_{SSF}	Ground
SDR LPSDRAM	
A0-A12	Row Address: RA0-RA11 Column Address: CA0-CA8 Auto-precharge flag: A10
BA0-BA1	Bank Address
DQ0-DQ15	Data Inputs/Outputs for x16 devices SDR_0
DQ16-DQ31	Data Inputs/Outputs for x16 devices SDR_1
K	Clock Input
KE	Clock Enable Input
$\overline{E}_{0D}$	Chip Select input for SDR_0
$\overline{E}_{1D}$	Chip Select input for SDR_1
$\overline{W}_D$	Write Enable Input
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
DQM0	Lower DQ Mask Enable Output for SDR_0
DQM1	Upper DQ Mask Enable Output for SDR_0
DQM2	Lower DQ Mask Enable Output for SDR_1
DQM3	Upper DQ Mask Enable Output for SDR_1
V_{DDD}	Supply Voltage
V_{DDQD}	Input/Output Supply Voltage
V_{SSD}	Ground
V_{SSQD}	Input/Output Ground
NC	Not Connected Internally

Figure 3. Logic Diagram: NAND Flash & DDR LPSDRAM

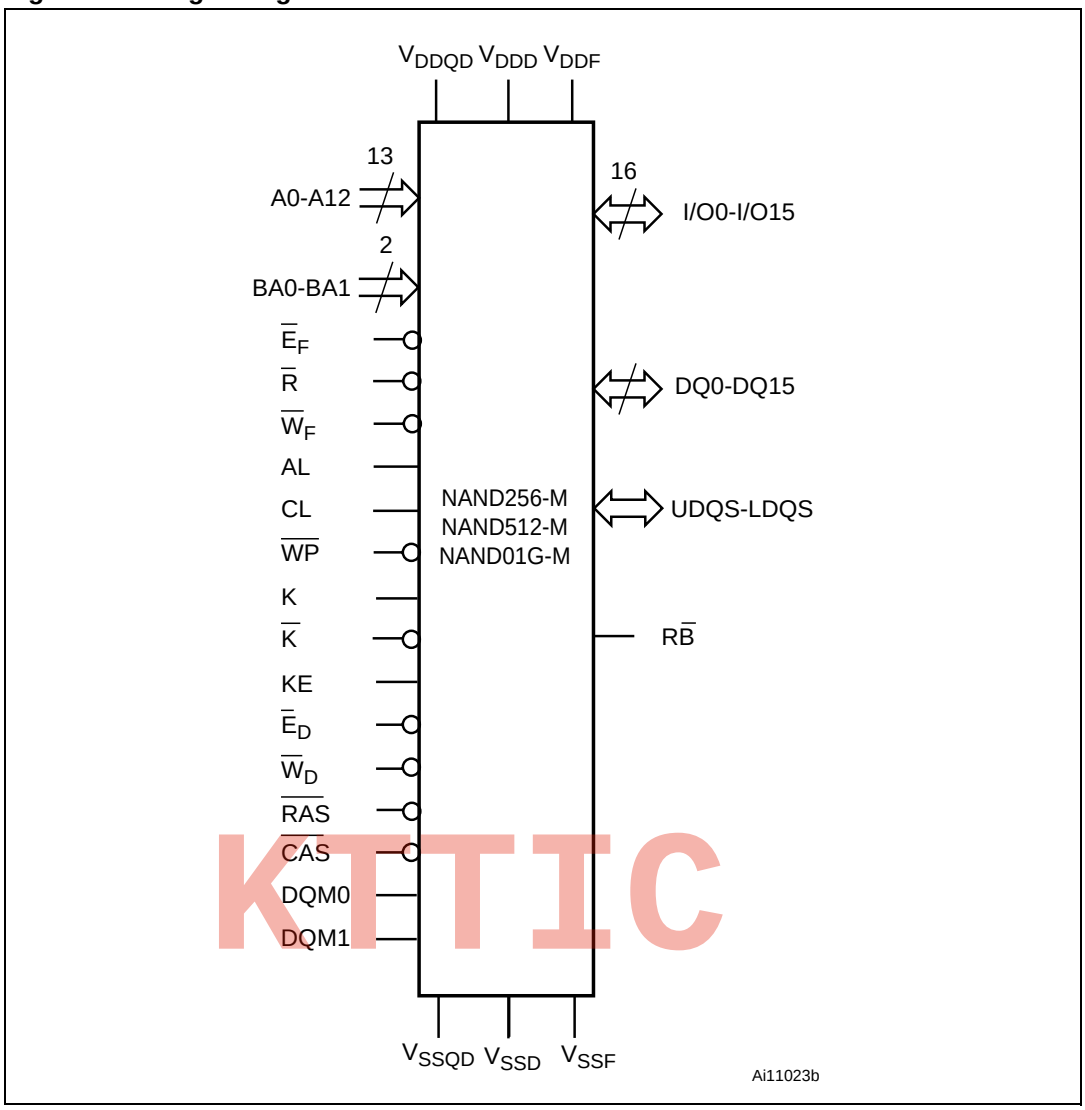


Table 4. Signal Names - NAND Flash & DDR LPSDRAM

NAND Flash	
I/O0-I/O15	Data Inputs/Outputs
AL	Address Latch Enable
CL	Command Latch Enable
$\overline{E}_F$	Chip Enable
R	Read Enable
R$\overline{B}$	Ready/Busy (open-drain output)
$\overline{W}_F$	Write Enable
$\overline{WP}$	Write Protect
V_{DDF}	Supply Voltage
V_{SSF}	Ground
DDR LPSDRAM	
A0-A12	Address Inputs A10 determines the Precharge mode.
BA0-BA1	Bank Select Inputs
DQ0-DQ15	Data Inputs/Outputs
UDQS-LDQS	Data Strobe Inputs/Outputs
K	Clock Input
$\overline{K}$	Clock Input
KE	Clock Enable Input
$\overline{E}_D$	Chip Select inputs
$\overline{W}_D$	Write Enable Input
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
DQM0	DQ Mask Enable Input (controls DQ0-DQ7)
DQM1	DQ Mask Enable Input (controls DQ8-DQ15)
V_{DDD}	Supply Voltage
V_{DDQD}	Input/Output Supply Voltage
V_{SSD}	Ground
V_{SSQD}	Input/Output Ground
NC	Not Connected Internally
DU	Do Not Use

Figure 4. TFBGA107 Connections (Top view through package)

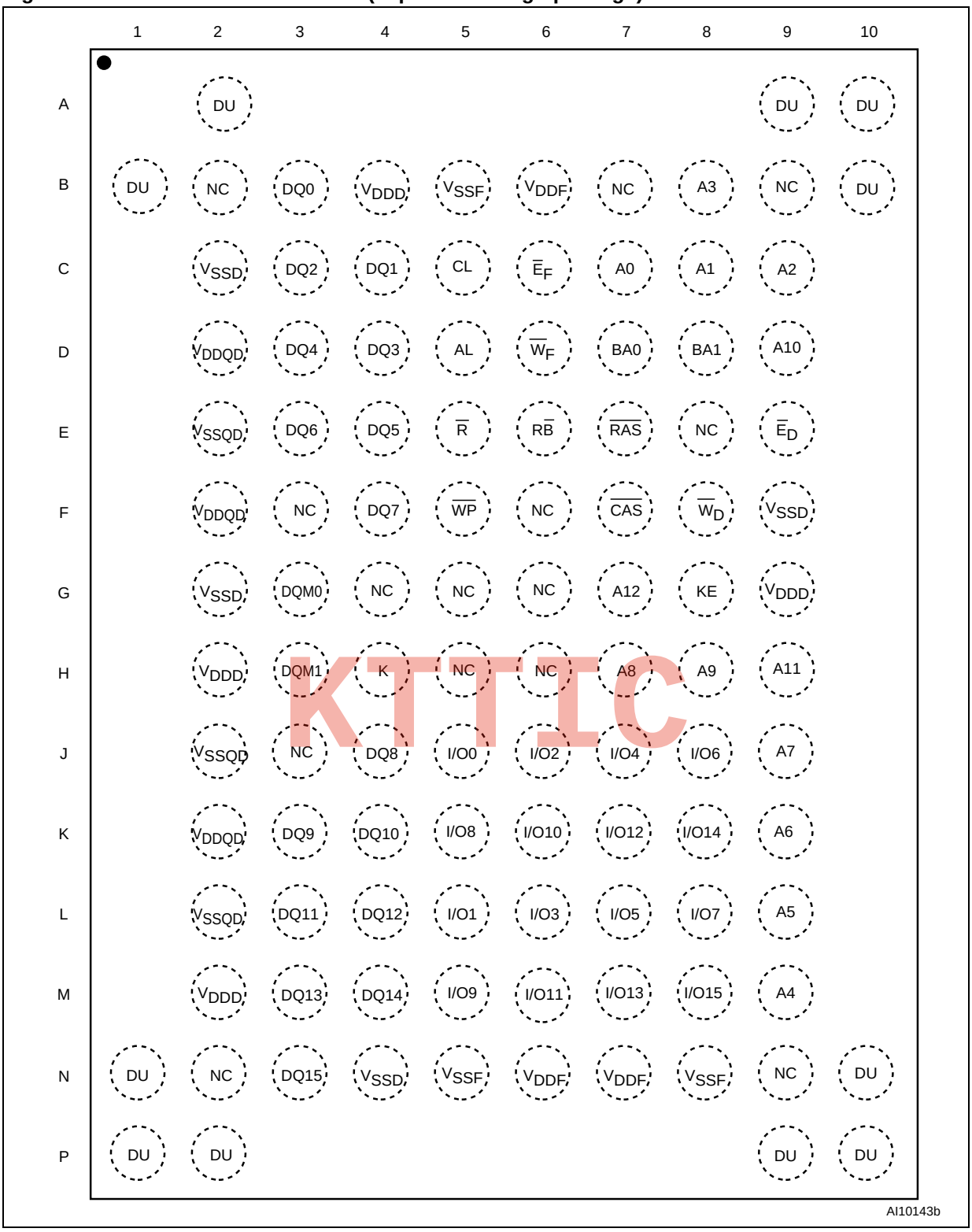
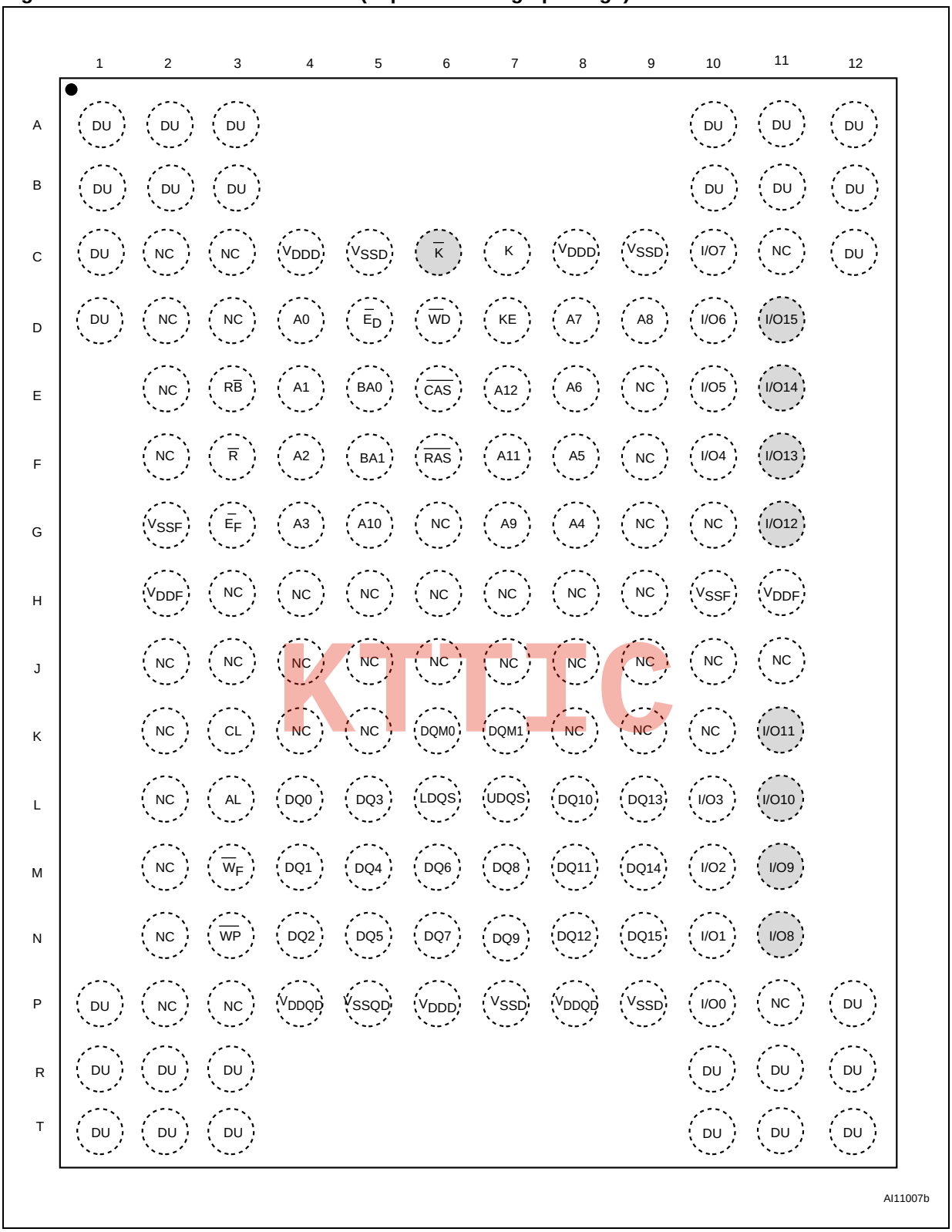
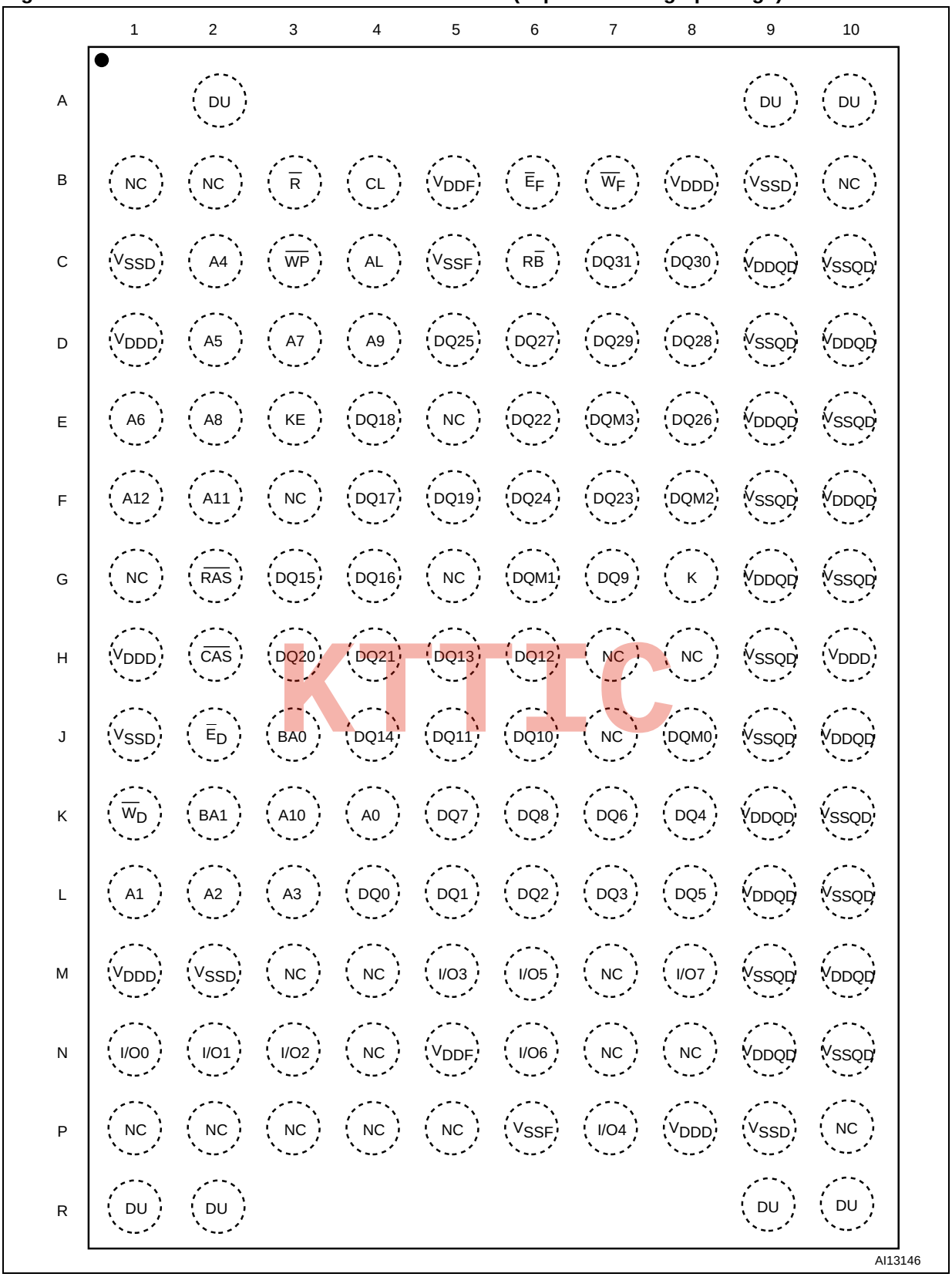


Figure 5. TFBGA149 Connections (Top view through package)



1. Balls shaded in gray are only present for NAND + DDR devices delivered in the TFBGA149 package.

Figure 6. LFBGA137 and TFBGA137 Connections (Top view through package)



2 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

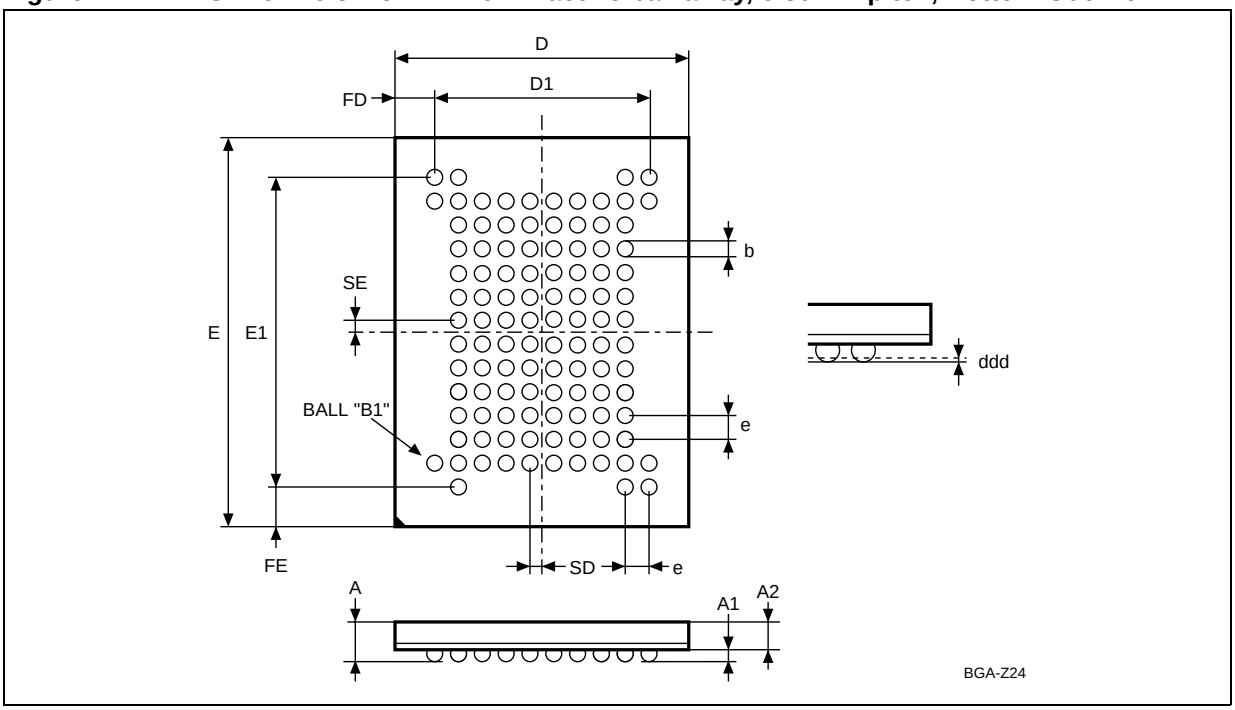
Table 5. Absolute Maximum Ratings

Symbol	Parameter		Value		Unit
			Min	Max	
T_A	Ambient Operating Temperature		-30	85	°C
T_{BIAS}	Temperature Under Bias		TBD(1)	TBD(1)	°C
T_{STG}	Storage Temperature		-55	125	°C
V_{IO}(2)	NAND Flash Input or Output Voltage	1.8V device	-0.6	2.7	V
		3V device	-0.6	4.6	V
	LPSDRAM Input or Output Voltage	1.8V device	-0.5	2.6	V
V_{DDF}	NAND Flash Supply Voltage	1.8V device	-0.6	2.7	V
		3V device	-0.6	4.6	V
V_{DDD}, V_{DDQD}	LPSDRAM Supply Voltage	1.8V device	-0.5	2.6	V
LPSDRAM Short Circuit Output Current	I_{OS}		50		mA
LPSDRAM Power Dissipation	PD		1.0		W

1. TBD stands for To Be Defined.
2. Minimum Voltage may undershoot to -2V for less than 20ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2V for less than 20ns during transitions on I/O pins.

3 Package Mechanical

Figure 7. TFBGA107 10.5x13mm - 10x14 active ball array, 0.80mm pitch, Bottom Outline



1. Drawing not to scale.

Table 6. TFBGA107 10.5x13mm - 10x14 active ball array, 0.80mm pitch, Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.25			0.010	
A2	0.80			0.031		
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.50	10.40	10.60	0.413	0.409	0.417
D1	7.20			0.283		
ddd			0.10			0.004
E	13.00	12.90	13.10	0.512	0.508	0.516
E1	10.40			0.409		
e	0.80	–	–	0.031	–	–
FD	1.65			0.065		
FE	1.30			0.051		
SD	0.40			0.016		
SE	0.40			0.016		

Figure 8. TFBGA149 10x13.5mm - 12x16 active ball array, 0.80mm pitch, Bottom Outline

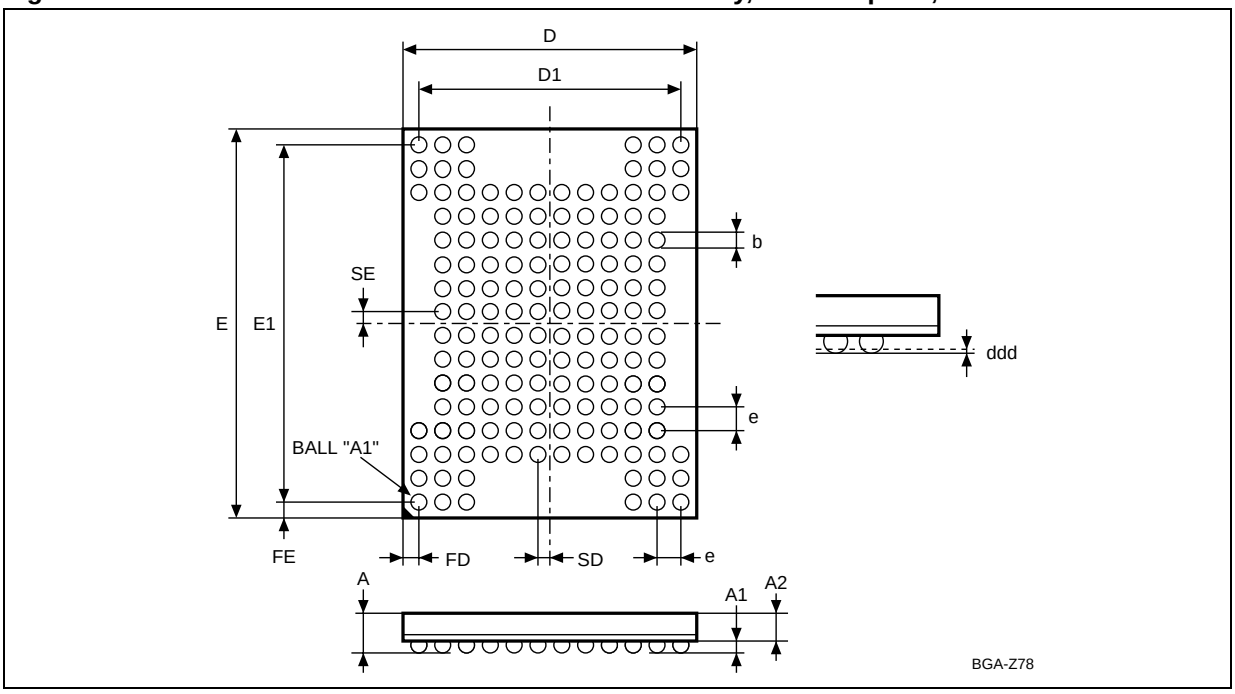
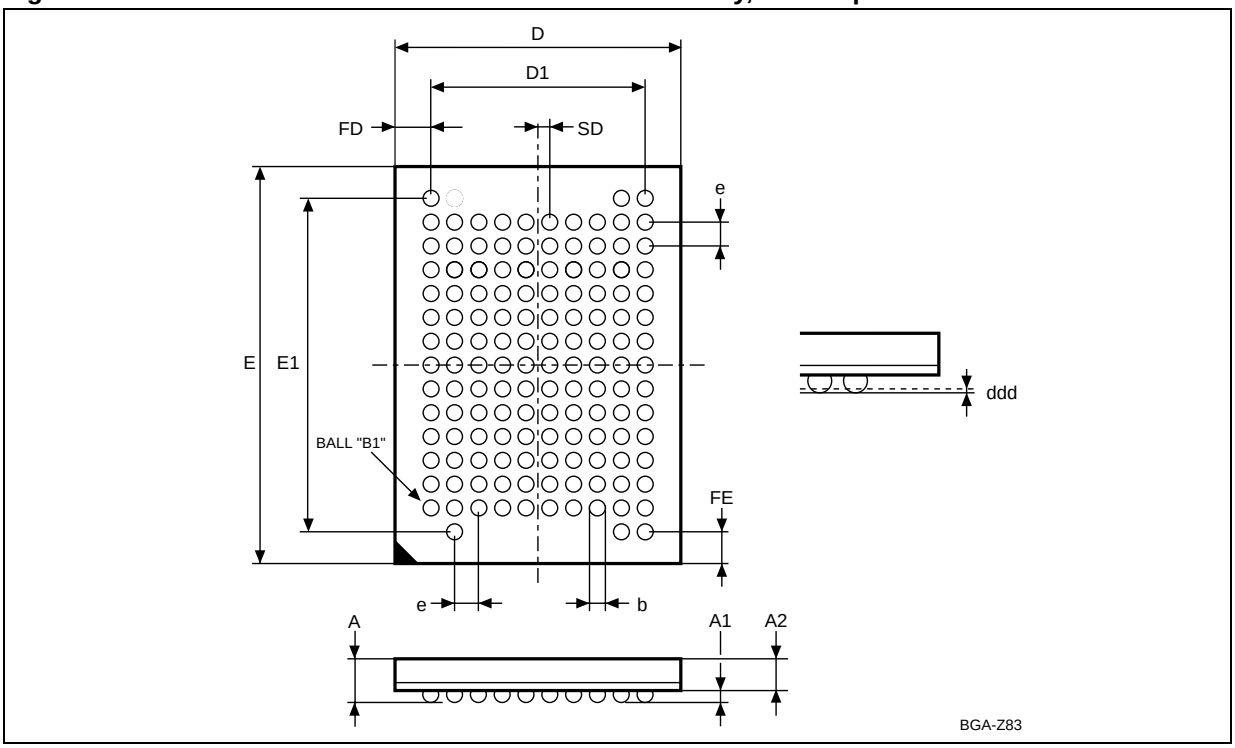


Table 7. TFBGA149 10x13.5mm - 12x16 active ball array, 0.80mm pitch, Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.250			0.0098	
A2	0.800			0.0315		
b	0.450	0.400	0.500	0.0177	0.0157	0.0197
D	10.000	9.900	10.100	0.3937	0.3898	0.3976
D1	8.800			0.3465		
ddd			0.100			0.0039
E	13.500	13.400	13.600	0.5315	0.5276	0.5354
E1	12.000			0.4724		
e	0.800	–	–	0.0315	–	–
FD	0.600			0.0236		
FE	0.750			0.0295		
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

Figure 9. LFBGA137 10.5x13mm - 10x13 active ball array, 0.8mm pitch- Bottom Outline



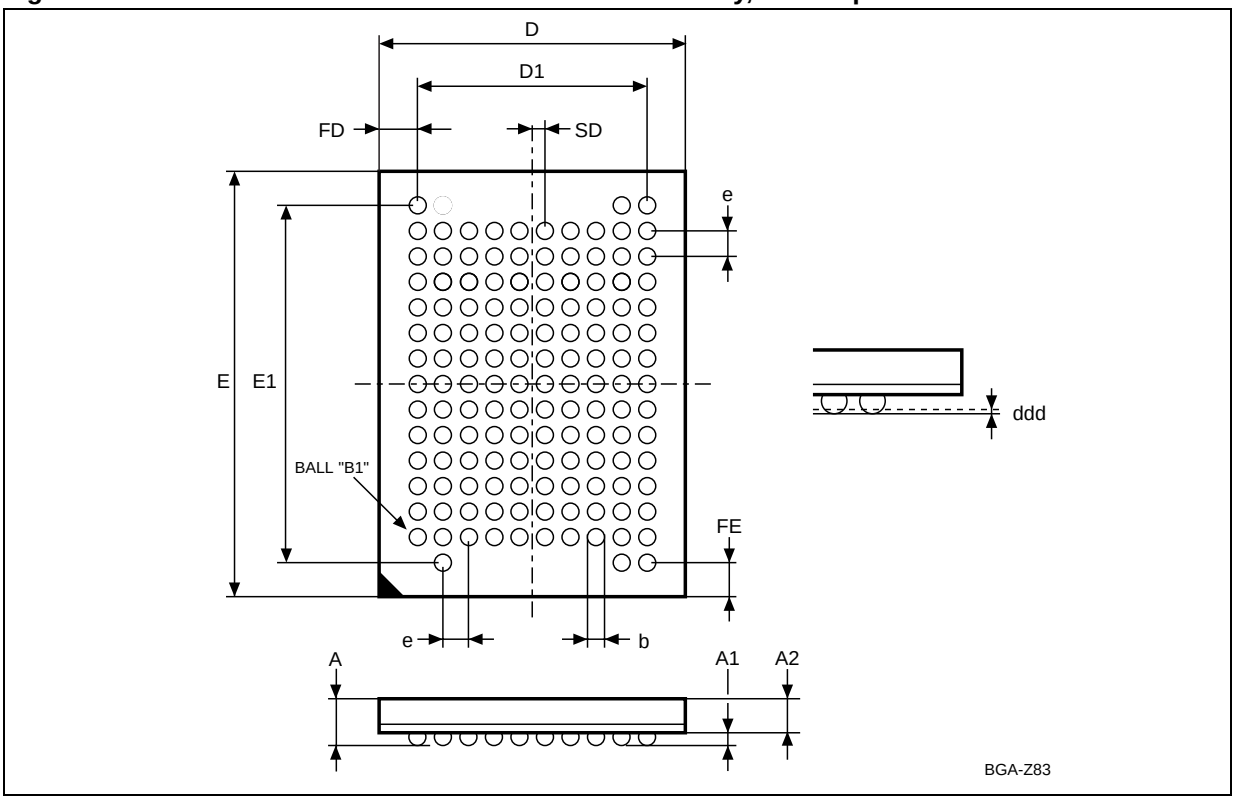
1. Subject to change without prior notice.

Table 8. LFBGA137 10.5x13mm - 10x13 active ball array, 0.8mm pitch- Mechanical Data(1)

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.40			0.055
A1		0.25			0.010	
A2	1.00			0.039		
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.50	10.40	10.60	0.413	0.409	0.417
D1	7.20			0.283		
ddd			0.10			0.004
E	13.00	12.90	13.10	0.512	0.508	0.516
E1	11.20			0.441		
e	0.80	–	–	0.031	–	–
FD	1.65			0.065		
FE	0.90			0.035		
SD	0.40			0.016		

1. Subject to change without prior notice.

Figure 10. TFBGA137 10.5x13mm - 10x13 active ball array, 0.8mm pitch- Bottom Outline



1. Subject to change without prior notice.

Table 9. TFBGA137 10.5x13mm - 10x13 active ball array, 0.80mm pitch

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.25			0.010	
A2	0.80			0.031		
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.50	10.40	10.60	0.413	0.409	0.417
D1	7.20			0.283		
E	13.00	12.90	13.10	0.512	0.508	0.516
E1	11.20			0.441		
e	0.80	–	–	0.031	–	–
FD	1.65			0.065		
FE	0.90			0.035		
SD	0.40	–	–	0.016	–	–

4 Part Numbering

Table 10. Ordering Information Scheme

Example: NAND256 R 3 M 4 A ZB 5 E

Device Type
NAND Flash Memory

NAND Flash Density
256 = 256Mb
512 = 512Mb
01G = 1Gb

Operating Voltage
R = V_{DDF} = 1.7V to 1.95V
W = V_{DDF} = 2.5V to 3.6V

NAND Bus Width
3 = x8
4 = x16

Family Identifier
M = 528 Byte Page NAND Flash + LPSDRAM

Device Options
0 = 256, x16, 104MHz, SDR, BGA107
2 = 2 x 256, 2x16, 104MHz, SDR, BGA137 or
512, x32, 133MHz, SDR, BGA137
3 = 256, x16, 133MHz, DDR BGA149
4 = 256, x16, 104MHz, SDR, BGA149
5 = 512, x16, 133MHz, DDR, BGA149

Product Version
A
B
C

Package
ZB = TFBGA
ZC = LFBGA

Temperature range
5 = -30°c to 85°C

Option
E = ECOPACK Package, Standard Packing
F = ECOPACK Package, Tape & Reel Packing

Devices are shipped from the factory with the Flash memory content bits, in valid blocks, erased to '1'. For further information on any aspect of this device, please contact your nearest ST Sales Office.

5 Revision history

Table 11. Document Revision History

Date	Version	Revision Details
06-Feb-2006	1.0	First Issue.
09-Feb-2006	2.0	Reference M65KG256AD changed to M65KG256AB.
07-Apr-2006	3	Part numbers NAND512R4M3 and NAND512R4M5 added, corresponding to 1 die of 512 Mb (x16) NAND Flash + 1 die of 256 Mb or 512 Mb (x16) DDR LPSDRAM.
23-May-2006	4	Temperature range -25 to 85°C removed for 512 Mbit LPSDRAMs. NAND512W3M2 part number added in *Table 1: Product List*. *Figure 5: TFBGA149 Connections (Top view through package)* updated. LPSDRAM supply voltage changed to 1.7 to 1.9V.
24-Aug-2006	5	1 Gbit (x8) 3V NAND Flash memory and 512Mbit SDR (x32) 1.8V, 133MHz LPSDRAM added for NAND01GW3M2. TFBGA137 package added.

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