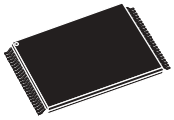
NAND04GA3C2A
NAND04GW3C2A

4Gbit, 2112 Byte Page, 3V, Multi-level NAND Flash Memory

Features

- High density multi-level Cell (MLC) NAND Flash memories:
  - Up to 128 Mbit spare area
  - Cost effective solutions for mass storage applications
- NAND interface
  - x8 bus width
  - Multiplexed Address/ Data
- Supply voltages
  - V_{DD} = 2.7 to 3.6V core supply voltage for Program, Erase and Read operations.
  - V_{DDQ} = 1.7 to 1.95 or 2.7 to 3.6V for I/O buffers.
- Page size: (2048 + 64 spare) Bytes
- Block size: (256K + 8K spare) Bytes
- Page Read/Program
  - Random access: 60µs (max)
  - Sequential access: 60ns(min)
  - Page Program Operation time: 800µs (typ)
- Cache Read mode
  - Internal Cache Register to improve the read throughput
- Fast Block Erase
  - Block erase time: 1.5ms (typ)
- Status Register
- Electronic Signature
- Serial Number option



TSOP48 12 x 20mm

- Chip Enable ‘don’t care’
  - for simple interface with microcontroller
- Data Protection
  - Hardware Program/Erase locked during power transitions
- Embedded Error Correction Code (ECC)
  - Internal ECC accelerator
  - Easy ECC Command Interface
- Data integrity
  - 10,000 Program/Erase cycles (with ECC)
  - 10 years Data Retention
- ECOPACK® package available
- Development tools
  - Bad Blocks Management and Wear Leveling algorithms
  - File System OS Native reference software
  - Hardware simulation models

Table 1. Product List

Reference	Part Number	Density
NAND04Gx3C2A	NAND04GA3C2A	4 Gbits
	NAND04GW3C2A	

Contents

List of tables

List of figures

1 Summary description

The NAND04GA3C2A and NAND04GW3C2A are a Multi-level Cell(MLC) devices from the NAND Flash 2112 Byte Page family of non-volatile Flash memories. The devices are offered in 1.8V and 3V V_{DDQ} I/O power supplies. The core voltage is 3V $V_{DD.}$ The size of a Page is 2112 Bytes (2048 + 64 spare).

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 Input/Output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 10,000 cycles. The devices also have hardware security features; a Write Protect pin is available to give hardware protection against Program and Erase operations.

The devices feature an open-drain Ready/Busy output that can be used to identify if the Program/Erase/Read (P/E/R) Controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor.

Each device has a Cache Read feature which improves the read throughput for large files. During Cache Reading, the device loads the data in a Cache Register while the previous data is transferred to the I/O Buffers to be read.

All devices have the Chip Enable Don't Care feature, which allows code to be directly downloaded by a microcontroller, as Chip Enable transitions during the latency time do not stop the read operation

There is the option of a Unique Identifier (serial number), which allows each device to be uniquely identified. It is subject to an NDA (Non Disclosure Agreement) and is therefore not described in the datasheet. For more details of this option contact your nearest ST Sales office.

The NAND04GA3C2A and NAND04GW3C2A are available in a TSOP48 (12 x 20mm) package. In order to meet environmental requirements, ST offers the devices in ECOPACK® packages. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

For information on how to order these options refer to *Table 22: Ordering Information Scheme*. Devices are shipped from the factory with Block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

See *Table 2: Product Description*, for all the devices available in the family.

Table 2. Product Description

Reference	Part Number	Density	Bus Width	Page Size	Block Size	Memory Array	Operating Voltage V_{DD}	Operating Voltage V_{DDQ}	Timings				Package
									Random Access (max)	Sequential Access (min)	Page Program (typ)	Block Erase (typ)	
NAND04Gx3C2A	NAND04GW3C2A	4Gbits	x8	2048+64 Bytes	256K+8K Bytes	128 Pages x 2048 Blocks	2.7 to 3.6V	2.7V to 3.6V	60µs	60ns	800µs	1.5ms	TSOP48
	NAND04GA3C2A						2.7 to 3.6V	1.7V to 1.95V					

Figure 1. Logic Block Diagram

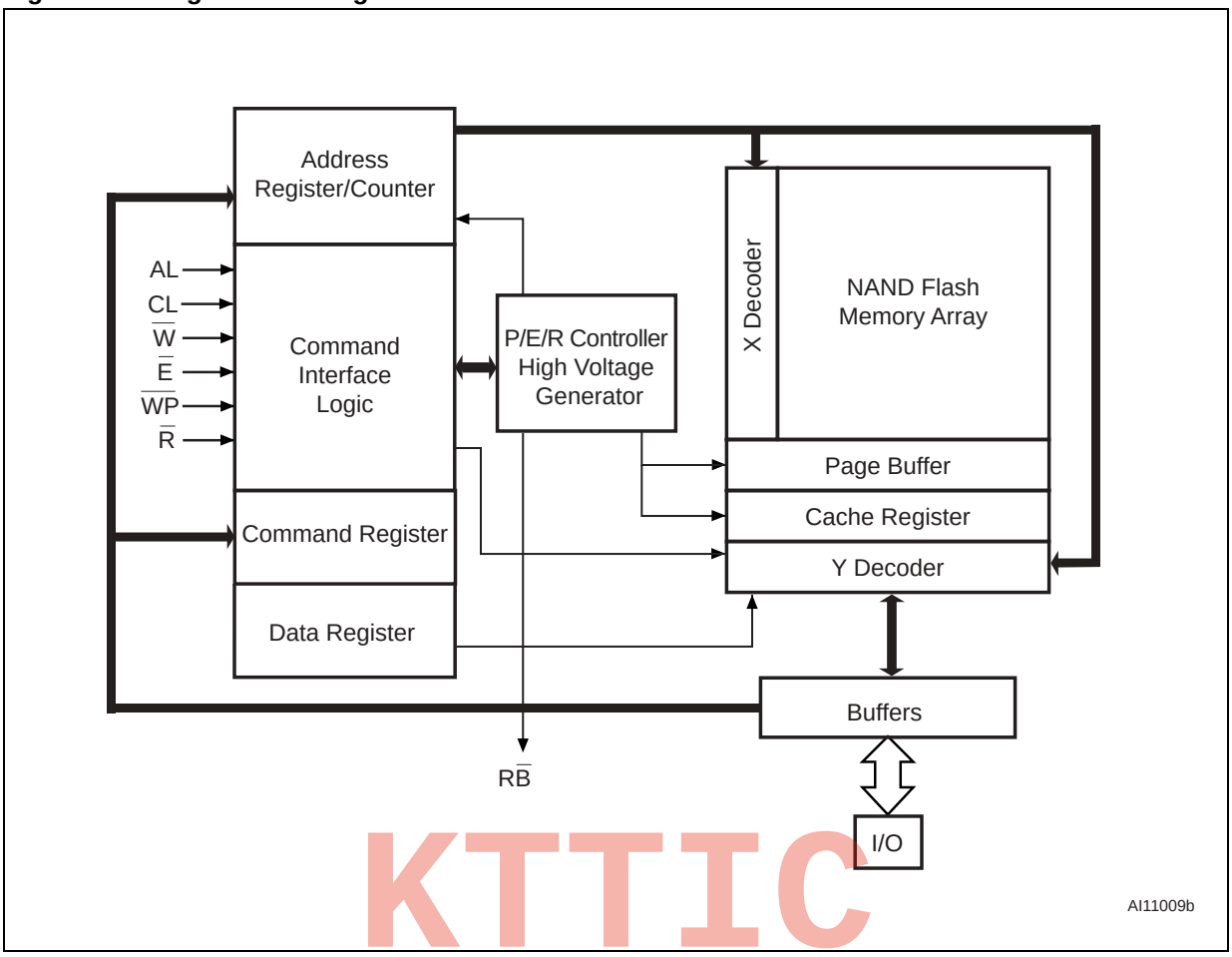


Figure 2. Logic diagram

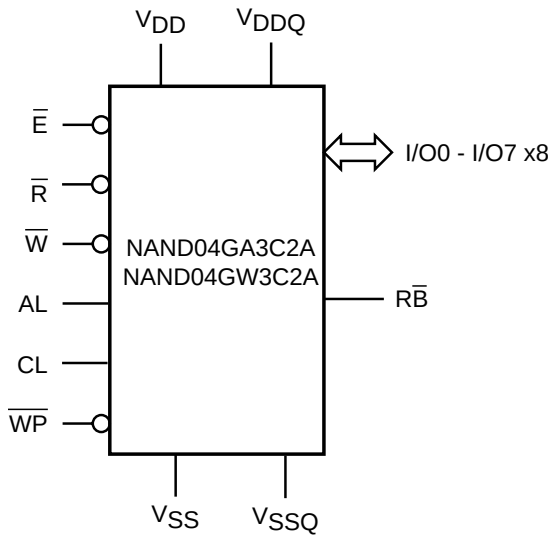
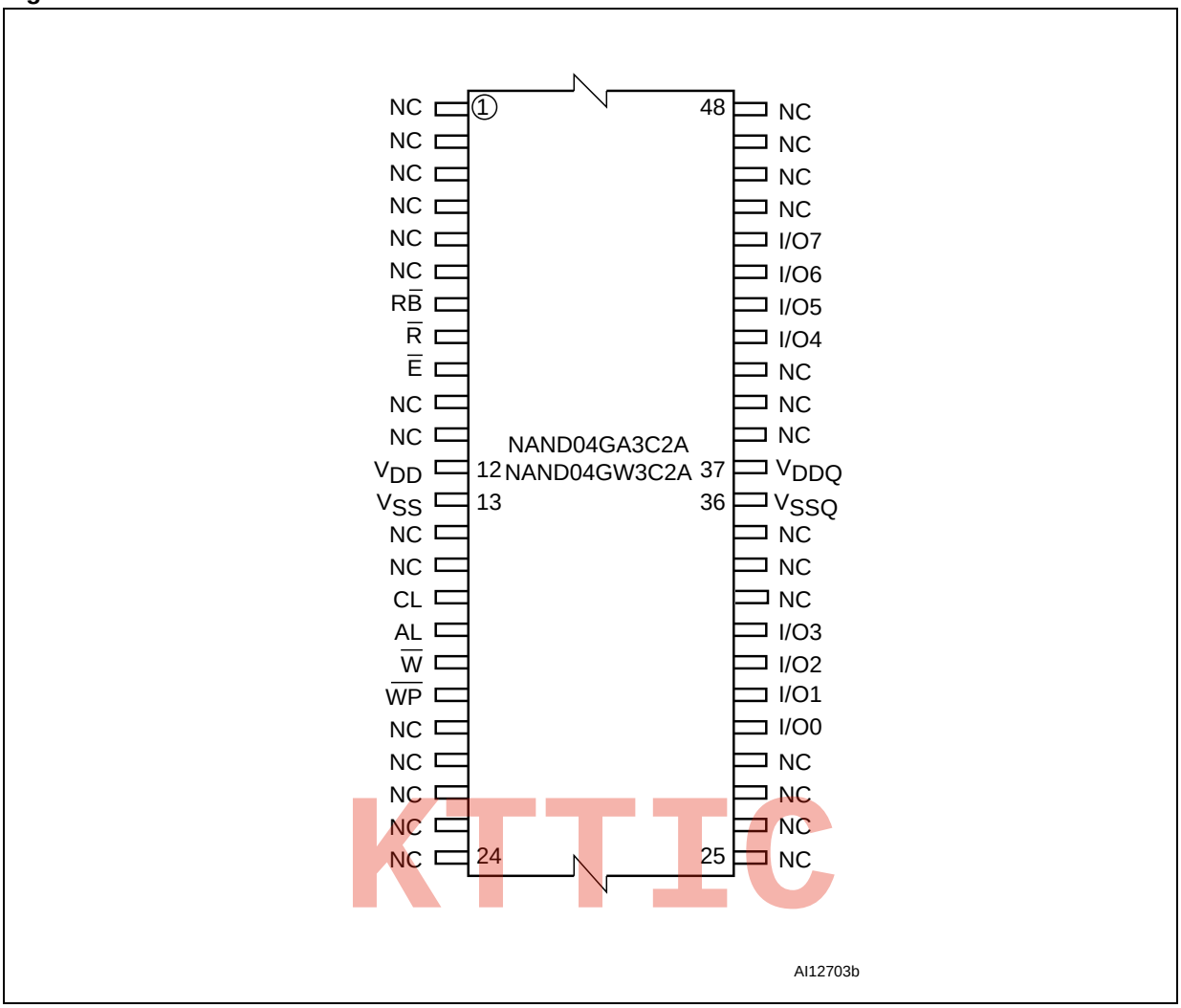


Table 3. Signal Names

I/O0 - I/O7	Data Input / Outputs
CL	Command latch enable
AL	Address latch enable
$\overline{E}$	Chip Enable
$\overline{R}$	Read Enable
$\overline{W}$	Write Enable
$\overline{WP}$	Write Protect
$R\overline{B}$	Ready / Busy (open drain output)
V_{DD}	Power supply
V_{DDQ}	I/O Power
V_{SS}	Ground
V_{SSQ}	I/O Ground
NC	No Connection
DU	Do Not Use

Figure 3. TSOP48 Connections x8 devices



2 Memory array organization

The memory array is made up of NAND structures where 32 cells are connected in series.

The memory array is organized in blocks where each block contains 128 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store software flags or Bad Block identification.

The pages are split into a 2048 Byte main area and a spare area of 64 Bytes.Refer to *Figure 4: Memory Array Organization*.

2.1 Bad blocks

The NAND04GA3C2A and NAND04GW3C2A devices may contain Bad Blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional Bad Blocks may develop during the lifetime of the device.

The Bad Block Information is written prior to shipping (refer to *Section 9.1: Bad block management* for more details).

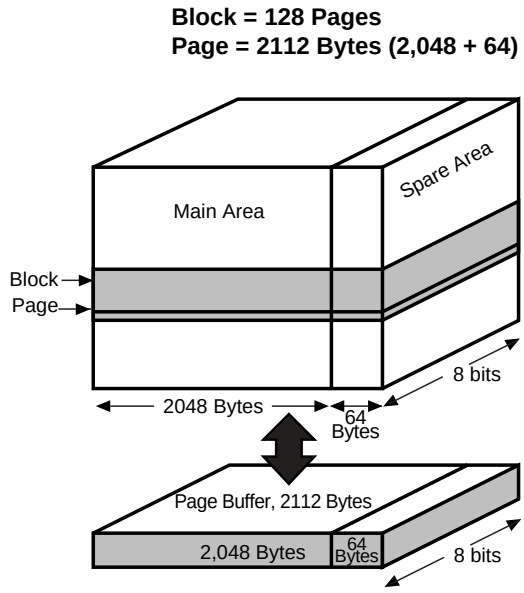
Table 4: Valid Blocks shows the minimum number of valid blocks in each device. The values shown include both the Bad Blocks that are present when the device is shipped and the Bad Blocks that could develop later on.

These blocks need to be managed using Bad Blocks Management and Block Replacement (refer to *Section 9: Software algorithms*).

Table 4. Valid Blocks

Density of Device	Min	Max
4 Gbits	2008	2048

Figure 4. Memory Array Organization



3 Signal Descriptions

See *Figure 1: Logic Block Diagram*, and *Table 3: Signal Names*, for a brief overview of the signals connected to this device.

3.1 Inputs/outputs (I/O0-I/O7)

Input/Outputs 0 to 7 are used to input the selected address, output the data during a Read operation or input a command or data during a Write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the Address inputs in the Command Interface. When AL is high, the inputs are latched on the rising edge of Write Enable.

3.3 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the Command inputs in the Command Interface. When CL is high, the inputs are latched on the rising edge of Write Enable.

3.4 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is low, V_{IL}, the device is selected. If Chip Enable goes high, v_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.5 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during Read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.6 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10µs (min) is required before the Command Interface is ready to accept a command. It is recommended to keep Write Enable high during the recovery time.

3.7 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.8 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the P/E/R Controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Refer to the *Section 12.1: Ready/busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.9 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for operations (read, program and erase).

3.10 V_{SS} ground

Ground, $V_{SS,}$ is the reference for the power supply. It must be connected to the system ground.

3.11 V_{SSQ}

V_{SSQ} is the ground reference for the I/O power supply. It must be connected to the system ground.

3.12 V_{DDQ}

V_{DDQ} provides power to the I/O buffers.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section, see *Table 5: Bus Operations*, for a summary.

Typically, glitches of less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command Input

Command Input bus operations are used to give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See *Figure 13* and *Table 19* for details of the timings requirements.

4.2 Address Input

Address Input bus operations are used to input the memory addresses. Five bus cycles are required to input the addresses (refer to *Table 6: Address insertion*).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

See *Figure 14* and *Table 19* for details of the timings requirements.

4.3 Data Input

Data Input bus operations are used to input the data to be programmed.

Data is only accepted when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 15* and *Table 19* for details of the timing requirements.

4.4 Data Output

Data Output Bus operations are used to read: the data in the memory array, the Status Register, the Electronic Signature and the Unique Identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

See *Figure 16* and *Table 20* for details of the timings requirements.

4.5 Write Protect

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations and so the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

4.6 Standby

The memory enters Standby mode by driving Chip Enable, $\overline{E}$, High. In standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 5. Bus Operations

Bus Operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7
Command Input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(1)	Command
Address Input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address
Data Input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data Input
Data Output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data Output
Write Protect	X	X	X	X	X	V_{IL}	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X

1. $\overline{WP}$ must be V_{IH} when issuing a Program or Erase command.

Table 6. Address insertion(1)

Bus Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A11	A10	A9	A8
3rd	A19	A18	A17	A16	A15	A14	A13	A12
4th	A27	A26	A25	A24	A23	A22	A21	A20
5th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A29	A28

1. Any additional address input cycles will be ignored.

Table 7. Address Definitions

Address	Definition
A0 - A11	Column Address
A12 - A18	Page Address
A19 - A29	Block Address

5 Command Set

All bus write operations to the device are interpreted by the Command Interface. The Commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is high. Device operations are selected by writing specific commands to the Command Register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The Commands are summarized in *Table 8: Commands*.

Table 8. Commands

Command	Bus Write Operations(1)				Commands accepted during busy
	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	
Read	00h(2)	30h	–	–	
Random Data Output	05h	E0h	–	–	
Cache Read	00h	31h	–	–	
Exit Cache Read	34h	–	–	–	Yes(3)
Page Program (Sequential Input default)	80h	10h	–	–	
Random Data Input	85h	–	–	–	
Block Erase	60h	D0h	–	–	
Reset	FFh	–	–	–	Yes
Read Electronic Signature	90h	–	–	–	
Read Status Register	70h	–	–	–	Yes

1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.
2. For consecutive read operations the 00h command does not need to be repeated.
3. Only when a Cache Read operation is ongoing.

6 Device operations

The following section gives the details of the device operations.

6.1 Read memory array

At Power-Up the device defaults to Read mode. To enter Read mode from another mode the Read command must be issued, see *Table 8: Commands*. Once a Read command is issued, subsequent consecutive Read commands only require the confirm command code (30h).

Once a Read command is issued two types of operations are available: Random Read and Page Read.

6.2 Random Read

Each time the Read command is issued the first read is Random Read.

6.3 Page read

After the first Random Read access, the page data (2112 Bytes) is transferred to the Page Buffer in a time of t_{WHBH} (refer to *Table 20* for value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

The device can output random data in a page, instead of the consecutive sequential data, by issuing a **Random Data Output command**.

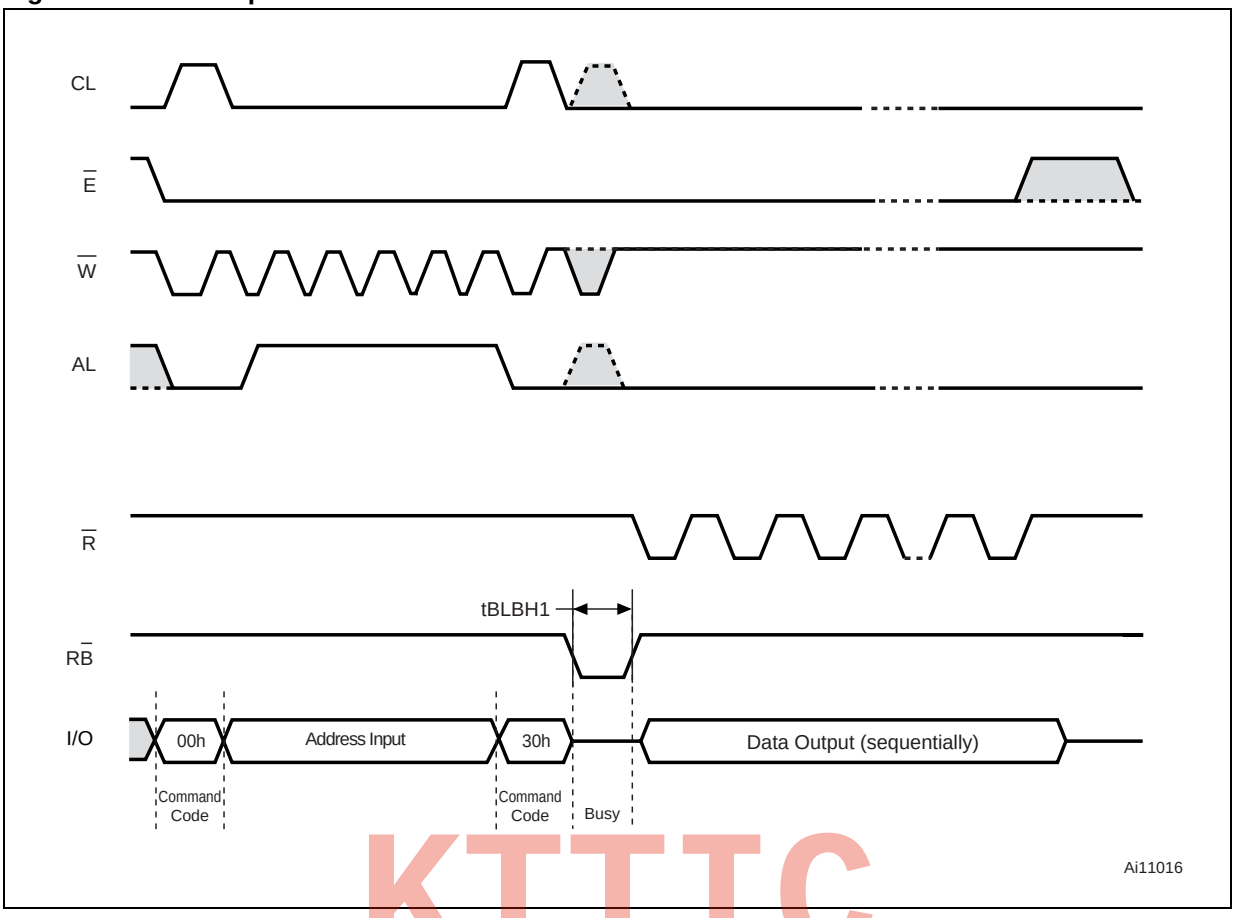
The Random Data Output command can be used to skip some data during a sequential data output.

The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command.

The Random Data Output command can be issued as many times as required within a page.

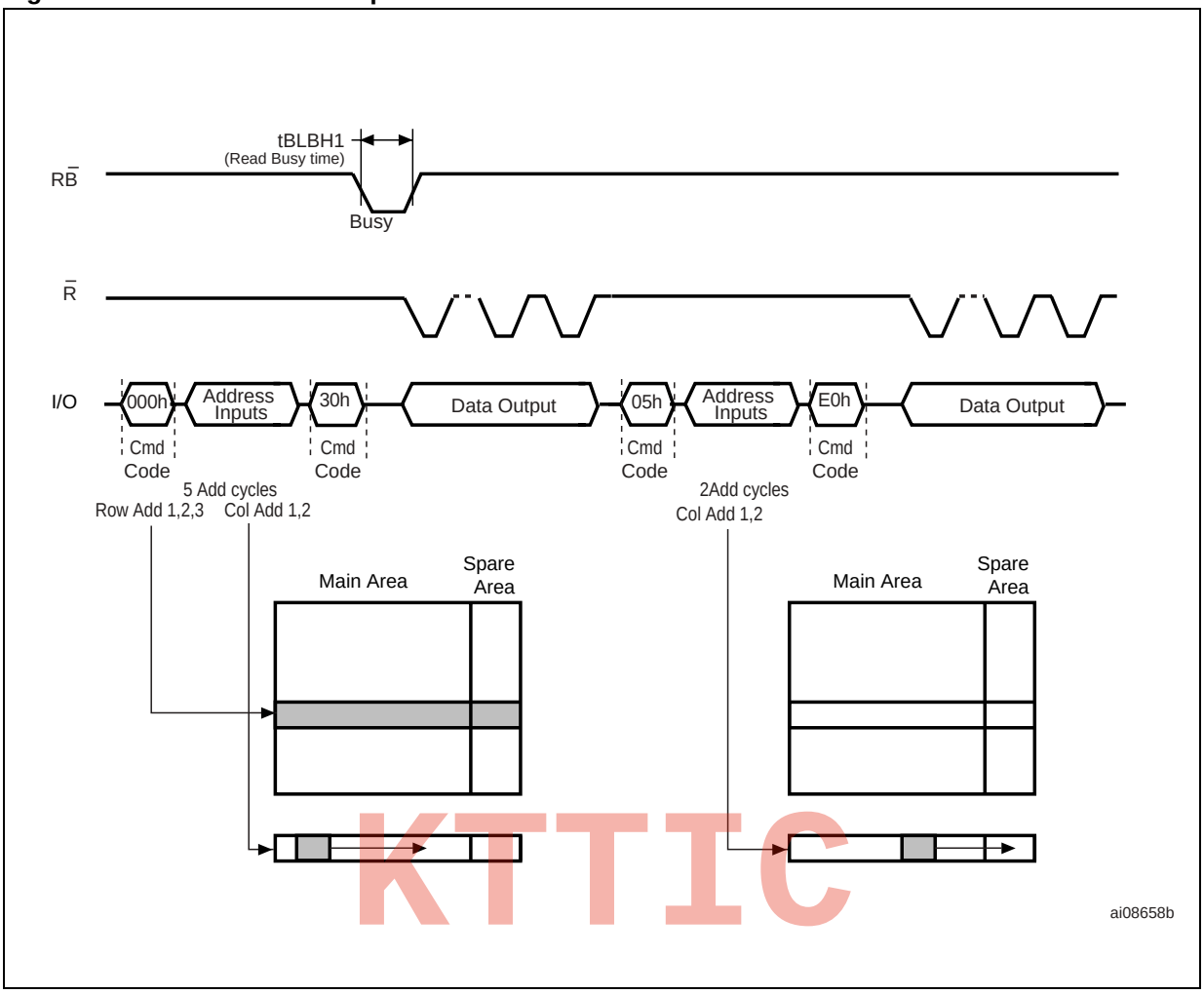
The Random Data Output command is not accepted during Cache Read operations.

Figure 5. Read Operations



1. Highest address depends on device density.

Figure 6. Random Data Output



6.4 Cache Read

The Cache Read operation is used to improve the read throughput by reading data using the Cache Register. As soon as the user starts to read one page, the device automatically loads the next page into the Cache Register.

An Cache Read operation consists of three steps (see *Table 8*):

1. One bus cycle is required to setup the Cache Read command (the same as the standard Read command).
2. Five bus cycles are then required to input the Start Address (refer to *Table 6*).
3. One bus cycle is required to issue the Cache Read confirm command to start the P/E/R Controller.

The Start Address must be at the beginning of a page (Column Address = 000h, see *Table 7.*). This allows the data to be output uninterrupted after the latency time (t_{BLBH1}), see *Figure 7.*

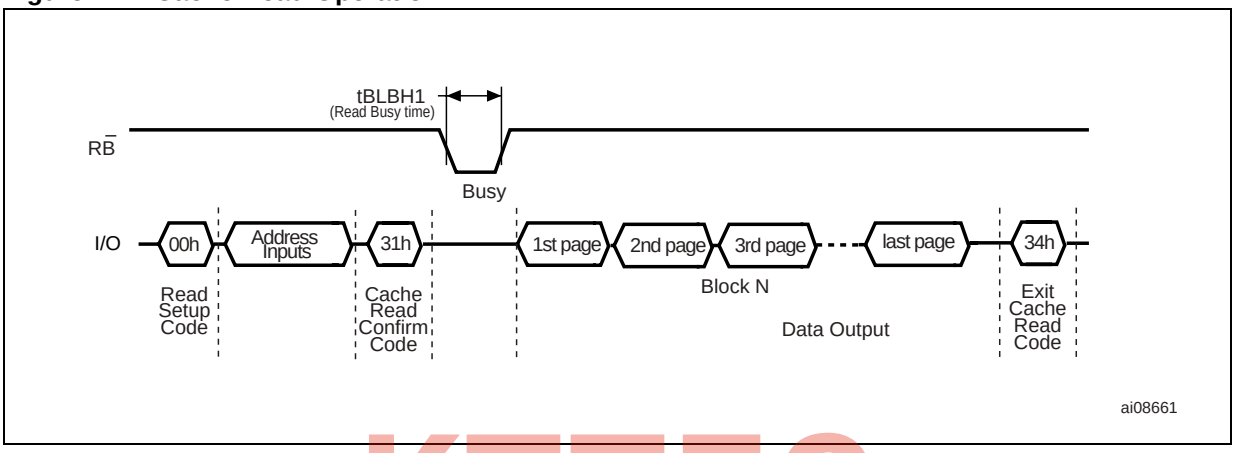
The Ready/Busy signal can be used to monitor the start of the operation. During the latency period the Ready/Busy signal goes Low, after this the Ready/Busy signal goes High, even if the device is internally downloading page n+1.

Once the Cache Read operation has started, the Status Register can be read using the Read Status Register command.

During the operation, SR5 can be read, to find out whether the internal reading is ongoing (SR5 = '0'), or has completed (SR5 = '1'), while SR6 indicates whether the Cache Register is ready to download new data.

To exit the Cache Read operation an Exit Cache Read command must be issued (see *Table 8*).

Figure 7. Cache Read Operation



6.5 Page Program

The Page Program operation is the standard operation to program data to the memory array. Generally, data is programmed sequentially, however the device does support Random Input within a page.

The memory array is programmed by page, however partial page programming is allowed where any number of Bytes (1 to 2112) can be programmed.

Only one consecutive partial page program operations is allowed on the same page. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page.

6.6 Sequential Input

To input data sequentially the addresses must be sequential and remain in one block.

For Sequential Input each Page Program operation comprises five steps:

1. One bus cycle is required to setup the Page Program (Sequential Input) command (see *Table 8*).
2. Five bus cycles are then required to input the program address (refer to *Table 6*).
3. The data is then loaded into the Data Registers.
4. One bus cycle is required to issue the Page Program confirm command to start the P/E/R Controller. The P/E/R will only start if the data has been loaded in step 3.
5. The P/E/R Controller then programs the data into the array.

6.7 Random Data input

During a Sequential Input operation, the next sequential address to be programmed can be replaced by a random address, by issuing a Random Data Input command. The following two steps are required to issue the command:

1. One bus cycle is required to setup the Random Data Input command (see *Table 8*).
2. Two bus cycles are then required to input the new column address (refer to *Table 6*).

Random Data Input can be repeated as often as required in any given page.

Once the program operation has started the Status Register can be read using the Read Status Register command. During program operations the Status Register will only flag errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R Controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High.

The device remains in Read Status Register mode until another valid command is written to the Command Interface.

Figure 8. Page Program Operation

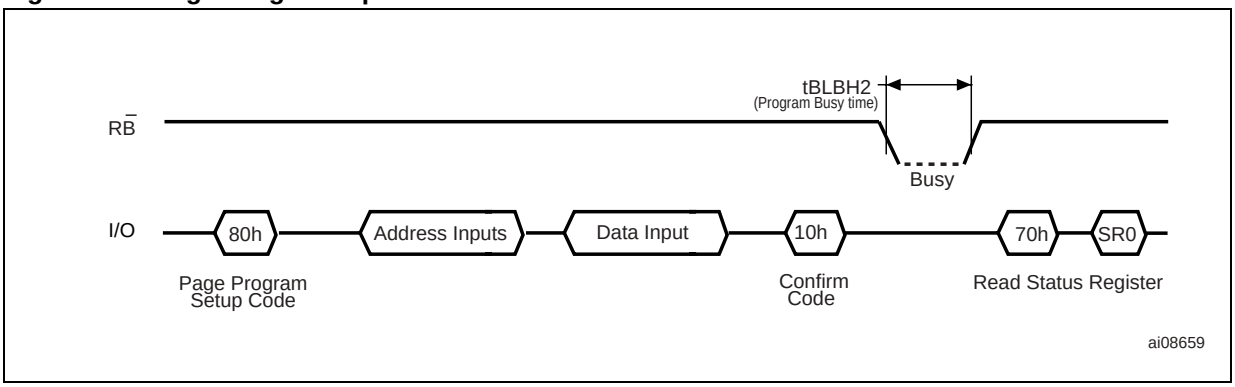
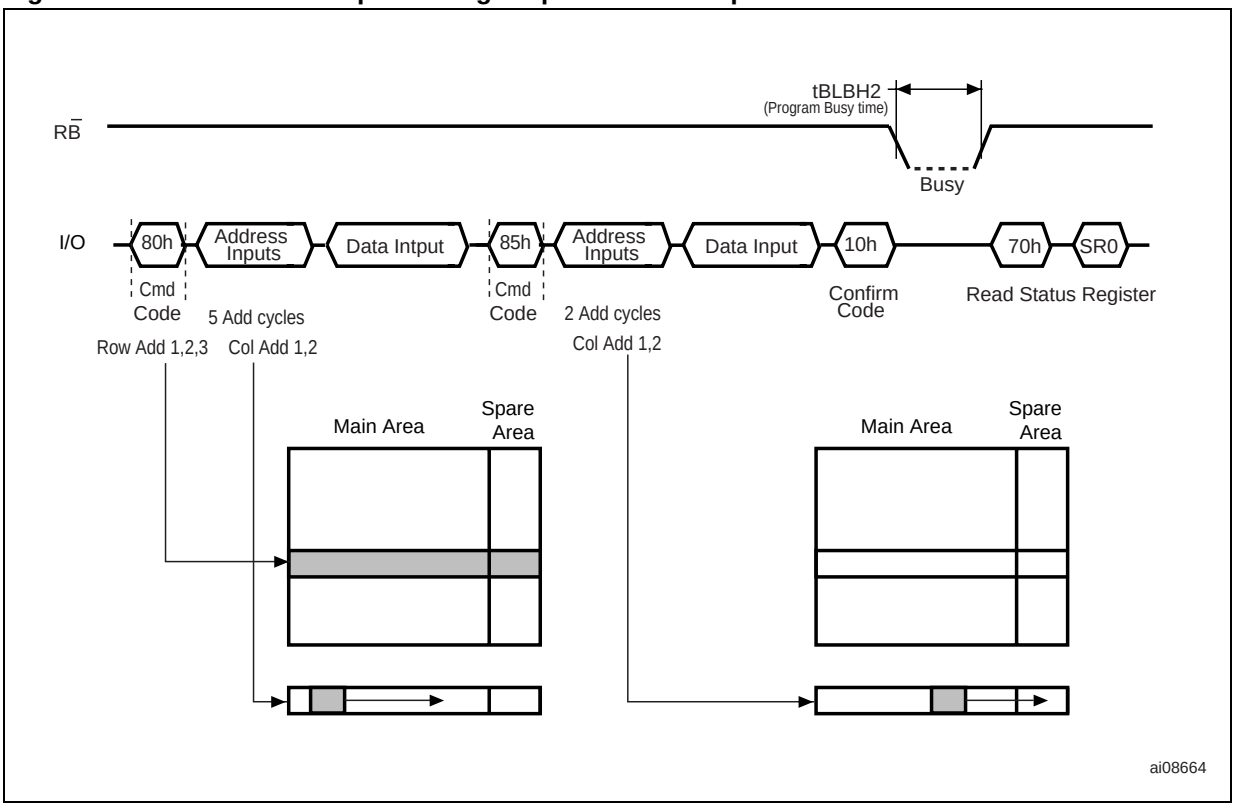


Figure 9. Random Data Input During Sequential Data Input



6.8 Block Erase

Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to ‘1’. All previous data in the block is lost.

An erase operation consists of three steps (refer to *Figure 10*:

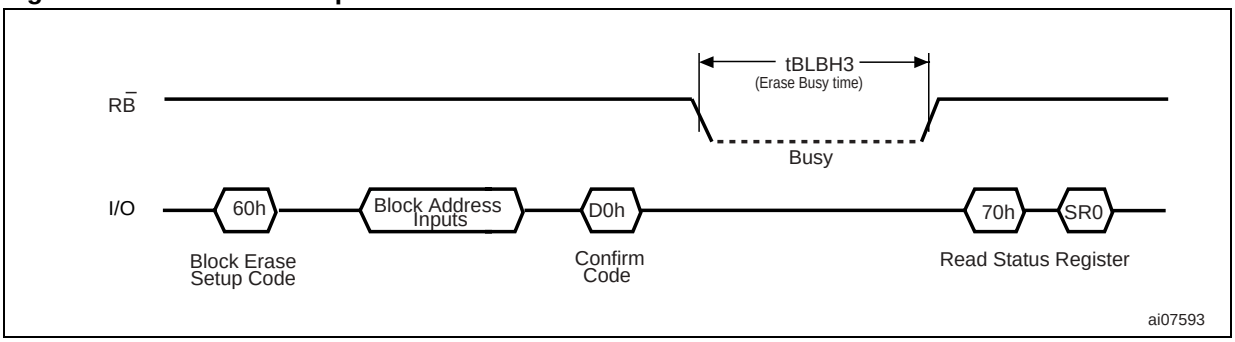
1. One bus cycle is required to setup the Block Erase command. Only addresses A19 to A30 are used, the other address inputs are ignored.
2. Three bus cycles are then required to load the address of the block to be erased. Refer to *Table 7* for the block addresses of each device.
3. One bus cycle is required to issue the Block Erase confirm command to start the P/E/R Controller.

The operation is initiated on the rising edge of write Enable, $\overline{W}$, after the confirm command is issued. The P/E/R Controller handles Block Erase and implements the verify process.

During the Block Erase operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R Controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High. If the operation completed successfully, the Write Status Bit SR0 is ‘0’, otherwise it is set to ‘1’.

Figure 10. Block Erase Operation



6.9 Reset

The Reset command is used to reset the Command Interface and Status Register. If the Reset command is issued during any operation, the operation will be aborted. If it was a program or erase operation that was aborted, the contents of the memory locations being modified will no longer be valid as the data will be partially programmed or erased.

If the device has already been reset then the new Reset command will not be accepted.

The Ready/Busy signal goes Low for t_{WHBH1} after the Reset command is issued. The value of t_{WHBH1} depends on the operation that the device was performing when the command was issued, refer to *Table 20* for the values.

6.10 Read Status Register

The device contains a Status Register which provides information on the current or previous Program or Erase operation. The various bits in the Status Register convey information and errors on the operation.

The Status Register is read by issuing the Read Status Register command. The Status Register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the Status Register.

After the Read Status Register command has been issued, the device remains in Read Status Register mode until another command is issued. Therefore if a Read Status Register command is issued during a Random Read cycle a new Read command must be issued to continue with a Page Read operation.

Refer to *Table 9* where Status Register bits are summarized. It should also be read in conjunction with the following text descriptions.

6.10.1 Write Protection Bit (SR7)

The Write Protection bit can be used to identify if the device is protected or not. If the Write Protection bit is set to '1' the device is not protected and program or erase operations are allowed. If the Write Protection bit is set to '0' the device is protected and program or erase operations are not allowed.

6.10.2 P/E/R Controller and Cache Ready/Busy Bit (SR6)

Status Register bit SR6 has two different functions depending on the current operation.

During Cache Read operations SR6 acts as a Cache Ready/Busy bit, which indicates whether the Cache Register is ready to accept new data. When SR6 is set to '0', the Cache Register is busy and when SR6 is set to '1', the Cache Register is ready to accept new data.

During all other operations SR6 acts as a P/E/R Controller bit, which indicates whether the P/E/R Controller is active or inactive. When the P/E/R Controller bit is set to ‘0’, the P/E/R Controller is active (device is busy); when the bit is set to ‘1’, the P/E/R Controller is inactive (device is ready).

6.10.3 P/E/R Controller Bit (SR5)

The Program/Erase/Read Controller bit indicates whether the P/E/R Controller is active or inactive. When the P/E/R Controller bit is set to ‘0’, the P/E/R Controller is active; when the bit is set to ‘1’, the P/E/R Controller is inactive.

6.10.4 Error Bit (SR0)

The Error bit is used to identify if any errors have been detected by the P/E/R Controller. The Error Bit is set to ’1’ when a program or erase operation has failed to write the correct data to the memory. If the Error Bit is set to ‘0’ the operation has completed successfully.

6.10.5 SR4, SR3, SR2 and SR1 are Reserved

Table 9. Status Register Bits

Bit	Name	Logic Level	Definition
SR7	Write Protection	'1'	Not Protected
		'0'	Protected
SR6(1)	Program/ Erase/ Read Controller	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
	Cache Ready/Busy	'1'	Cache Register ready (Cache Read only)
		'0'	Cache Register busy (Cache Read only)
SR5	Program/ Erase/ Read Controller(2)	'1'	P/E/R C inactive
		'0'	P/E/R C active
SR4, SR3, SR2, SR1	Reserved	Don't Care	
SR0(1)	Generic Error	'1'	Error – operation failed
		'0'	No Error – operation successful

1. The SR6 bit and SR0 bit have a different meaning during Cache Read operations.
2. Only valid for Cache Read operations, for other operations it is same as SR6.

6.11 Read Electronic Signature

The device contains a Manufacturer Code and Device Code. To read these codes three steps are required:

1. One Bus Write cycle to issue the Read Electronic Signature command (90h)
2. One Bus Write cycle to input the address (00h)
3. Four Bus Read Cycles to sequentially output the data (as shown in *Table 10: Electronic Signature*).

Table 10. Electronic Signature

Part Number	Byte/Word 1	Byte/Word 2	Byte 3 (see *Table 11*)	Byte 4 (see *Table 12*)
	Manufacturer Code	Device code		
NAND04GA3C2A	20h	DCh	84h	25h
NAND04GW3C2A	20h	DCh	84h	

Table 11. Electronic Signature Byte 3

I/O	Definition	Value	Description
I/O1-I/O0	Internal Chip number	0 0 0 1 1 0 1 1	1 2 4 8
I/O3-I/O2	Cell Type	0 0 0 1 1 0 1 1	2-level cell 4-level cell 8-level cell 16-level cell
I/O5-I/O4	Number of simultaneously programmed pages	0 0 0 1 1 0 1 1	1 2 4 8
I/O7-I/O6	Reserved	10	

Table 12. Electronic Signature Byte 4

I/O	Definition	Value	Description
I/O1-I/O0	Page size (Without Spare Area)	0 0 0 1 1 0 1 1	1 KBytes 2 KBytes Reserved Reserved
I/O2	Spare area size (Byte / 512 Byte)	0 1	8 16
I/O7, I/O3	Minimum sequential access time	0 0 1 0 0 1 1 1	50ns 30ns Reserved Reserved
I/O5-I/O4	Block size (without Spare Area)	0 0 0 1 1 0 1 1	64 KBytes 128 KBytes 256 KBytes Reserved
I/O6	Organization	0 1	x8 x16

7 Data Protection

The device has hardware features to protect against Program and Erase operations.

It features a Write Protect, $\overline{WP}$, pin, which can be used to protect the device against program and erase operations. It is recommended to keep $\overline{WP}$ at V_{IL} during power-up and power-down.

8 Embedded ECC accelerator

The NAND04GA3C2A and NAND04GW3C2A devices include a powerful embedded Error Correction Code (ECC) accelerator. This feature ensures high memory reliability and fast data throughput while simplifying the design of the memory application.

If the embedded ECC accelerator cannot be used, it is strongly recommended to use an external hardware accelerator to maintain the same data throughput. If this proves to be impossible, a software ECC can be implemented. However, this solution will result in lower performance compared to the hardware ECC solution.

The ECC operation and command set are described in a dedicated application note. Please contact the nearest STMicroelectronics sales office for further details.

9 Software algorithms

This section gives information on the software algorithms that ST recommends to implement to manage the Bad Blocks and extend the lifetime of the NAND device.

NAND Flash memories are programmed and erased by Fowler-Nordheim tunneling using a high voltage. Exposing the device to a high voltage for extended periods can cause the oxide layer to be damaged. For this reason, the number of program and erase cycles is limited (see *Table 14* for value) and it is recommended to implement Garbage Collection, Wear-Leveling and Error Correction Code algorithms to extend the number of program and erase cycles and increase the data retention.

To help integrate a NAND memory into an application ST Microelectronics can provide a File System OS Native reference software, which supports the basic commands of file management.

Contact the nearest ST Microelectronics sales office for more details.

9.1 Bad block management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block, where the 1st Byte in the spare area of the last page, does not contain FFh, is a Bad Block.

The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in *Figure 11.*

9.2 Block replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Refer to *Table 13* for the recommended procedure to follow if an error occurs during an operation.

Table 13. Block Failure

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement or ECC(1)
Read	ECC(1)

1. Example: 4 bit correction per 528 Bytes.

Figure 11. Bad Block Management Flowchart

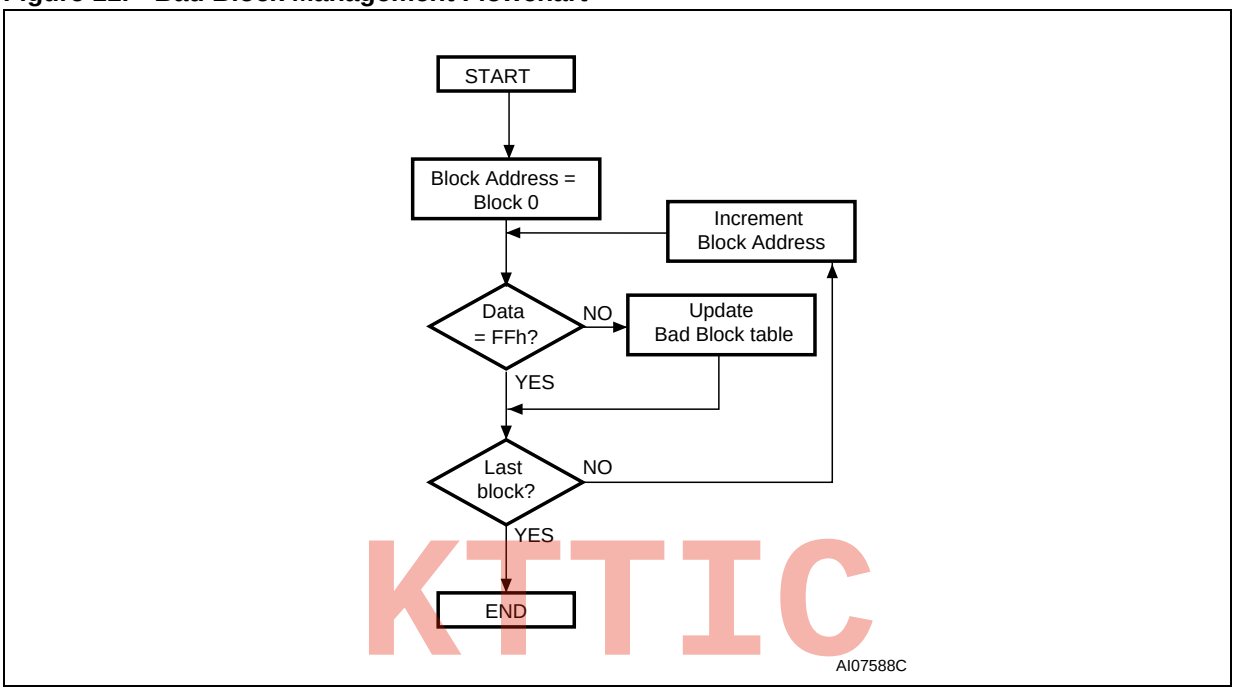
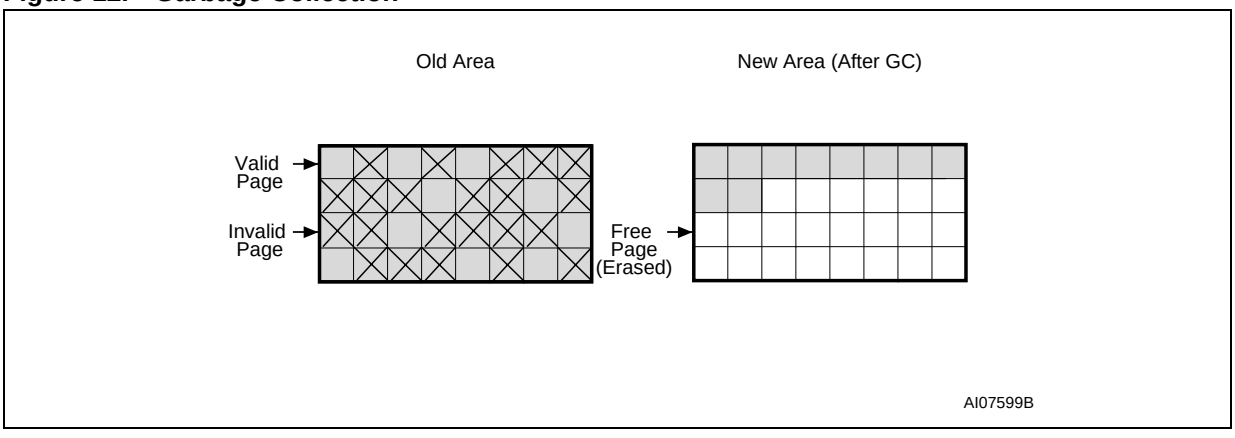


Figure 12. Garbage Collection



9.3 Garbage collection

When a data page needs to be modified, it is faster to write to the first available page, and the previous page is marked as invalid. After several updates it is necessary to remove invalid pages to free some memory space.

To free this memory space and allow further program operations it is recommended to implement a Garbage Collection algorithm. In a Garbage Collection software the valid pages are copied into a free area and the block containing the invalid pages is erased (see *Figure 12*).

9.4 Wear-leveling algorithm

For write-intensive applications, it is recommended to implement a Wear-leveling Algorithm to monitor and spread the number of write cycles per block.

In memories that do not use a Wear-Leveling Algorithm not all blocks get used at the same rate. Blocks with long-lived data do not endure as many write cycles as the blocks with frequently-changed data.

The Wear-leveling Algorithm ensures that equal use is made of all the available write cycles for each block. There are two wear-leveling levels:

1. First Level Wear-leveling, new data is programmed to the free blocks that have had the fewest write cycles
2. Second Level Wear-leveling, long-lived data is copied to another block so that the original block can be used for more frequently-changed data.

The Second Level Wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

9.5 Hardware simulation models

9.5.1 Behavioral simulation models

Denali Software Corporation models are platform independent functional models designed to assist customers in performing entire system simulations (typical VHDL/Verilog). These models describe the logic behavior and timings of NAND Flash devices, and so allow software to be developed before hardware.

9.5.2 IBIS simulations models

IBIS (I/O Buffer Information Specification) models describe the behavior of the I/O buffers and electrical characteristics of Flash devices.

These models provide information such as AC characteristics, rise/fall times and package mechanical data, all of which are measured or simulated at voltage and temperature ranges wider than those allowed by target specifications.

IBIS models are used to simulate PCB connections and can be used to resolve compatibility issues when upgrading devices. They can be imported into SPICETOOLS.

10 Program and erase times and endurance cycles

The Program and Erase times and the number of Program/ Erase cycles per block are shown in *Table 14*

Table 14. Program, Erase Times and Program Erase Endurance Cycles

Parameters	NAND04GA3C2A, NAND04GW3C2A			Unit
	Min	Typ	Max	
Page Program Time		800	2000	µs
Block Erase Time		1.5	3	ms
Program/Erase Cycles (per block)	10,000			cycles
Data Retention	10			years

11 Maximum rating

Stressing the device above the ratings listed in *Table 15: Absolute Maximum Ratings*, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 15. Absolute Maximum Ratings

Symbol	Parameter		Value		Unit
			Min	Max	
T_{BIAS}	Temperature Under Bias		– 50	125	°C
T_{STG}	Storage Temperature		– 65	150	°C
V_{IO}(1)	Input or Output Voltage	1.8V, V_{DDQ} devices	– 0.6	2.7	V
		3 V, V_{DDQ} devices	– 0.6	4.6	V
V_{DD}	Supply Voltage		– 0.6	4.6	V

1. Minimum Voltage may undershoot to –2V for less than 20ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2V for less than 20ns during transitions on I/O pins.

12 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 16: Operating and AC Measurement Conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

The DC and AC characteristics for V_{DDQ} 1.8V devices are not yet available.

Table 16. Operating and AC Measurement Conditions

Parameter		NAND04GA3C2A, NAND04GW3C2A		Units
		Min	Max	
Supply Voltage (V_{DD})	**1.8V, V_{DDQ} devices**	1.7	1.95	V
	3V, V_{DDQ} devices	2.7	3.6	V
Ambient Temperature (T_A)	**Grade 1**	0	70	°C
	Grade 6	–40	85	°C
Load Capacitance (C_L) (1 TTL GATE and C_L)	**1.8V V_{DDQ} devices**	30		pF
	3V, V_{DDQ} devices (2.7 - 3.6V)	50		pF
Input Pulses Voltages	**1.8V, V_{DDQ} devices**	0	V_{DD}	V
	3V, V_{DDQ} devices	0.4	2.4	V
Input and Output Timing Ref. Voltages	**1.8V, V_{DDQ} devices**	0.9		V
	3V, V_{DDQ} devices	1.5		V
Output Circuit Resistor R_{ref}		8.35		kΩ
Input Rise and Fall Times		5		ns

Table 17. Capacitance(1)

Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
$C_{I/O}$	Input/Output Capacitance	V_{IL} = 0V		10	pF

1. T_A = 25°C, f = 1 MHz. C_{IN} and $C_{I/O}$ are not 100% tested.

Table 18. DC Characteristics, V_{DDQ} 3V Devices(1)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
I_{DD1}	Operating Current	Sequential Read	t_{RLRL} minimum $\overline{E}=V_{IL}$, I_{OUT} = 0 mA	-	10	20	mA
I_{DD2}		Program	-	-	20	30	mA
I_{DD3}		Erase	-	-	15	20	mA
I_{DD4}	Standby current (TTL)		E=V_{IH}, $\overline{WP}$=0/V_{DD}			1	mA
I_{DD5}	Standby Current (CMOS)		$\overline{E}=V_{DD}$-0.2, $\overline{WP}$=0/V_{DD}	-	10	50	µA
I_{LI}	Input Leakage Current		V_{IN}= 0 to 3.6V	-	-	±10	µA
I_{LO}	Output Leakage Current		V_{OUT}= 0 to 3.6V	-	-	±10	µA
V_{IH}	Input High Voltage		-	2.0	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-	-0.3	-	0.8	V
V_{OH}	Output High Voltage Level		I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output Low Voltage Level		I_{OL} = 2.1mA	-	-	0.4	V
I_{OL} ($R\overline{B}$)	Output Low Current ($R\overline{B}$)		V_{OL} = 0.4V	8	10		mA

1. DC Characteristics for V_{DDQ} 1.8V devices are still to be determined.

Table 19. AC Characteristics for Command, Address, Data Input, V_{DDQ} 3V Devices(1)

Symbol	Alt. Symbol	Parameter			3V I/O	Unit
t_{ALLWH}	t_{ALS}	Address Latch Low to Write Enable High	AL Setup time	Min	40	ns
t_{ALHWH}		Address Latch High to Write Enable High				
t_{CLHWH}	t_{CLS}	Command Latch High to Write Enable High	CL Setup time	Min	20	ns
t_{CLLWH}		Command Latch Low to Write Enable High				
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data Setup time	Min	20	ns
t_{ELWH}	t_{CS}	Chip Enable Low to Write Enable High	$\overline{E}$ Setup time	Min	30	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL Hold time	Min	15	ns
t_{WHALL}		Write Enable High to Address Latch Low				
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	10	ns
t_{WHCLL}		Write Enable High to Command Latch Low				
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data Hold time	Min	15	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ Hold time	Min	10	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ High Hold time	Min	20	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ Pulse Width	Min	40	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write Cycle time	Min	60	ns

1. AC Characteristics for V_{DDQ} 1.8V devices are still to be determined.

Table 20. AC Characteristics for Operations, V_{DDQ} 3V Devices(1)

Symbol	Alt. Symbol	Parameter			3V I/O	Unit
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read Electronic Signature	Min	20	ns
t_{ALLRL2}			Read cycle	Min	20	ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		Min	20	ns
t_{BLBH1}		Ready/Busy Low to Ready/Busy High	Read Busy time	Max	60	µs
t_{BLBH2}	t_{PROG}		Program Busy time	Max	2000	µs
t_{BLBH3}	t_{BERS}		Erase Busy time	Max	3	ms
t_{BLBH4}			Reset Busy time, during ready	Max	5	µs
t_{WHBH1}	t_{RST}	Write Enable High to Ready/Busy High	Reset Busy time, during read	Max	20	µs
			Reset Busy time, during program	Max	40	µs
			Reset Busy time, during erase	Max	200	µs
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		Min	15	ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		Min	0	ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z		Max	30	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid		Max	50	ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High Hold time	Min	20	ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-Z		Max	30	ns
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable Pulse Width	Min	40	ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read Cycle time	Min	60	ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable Access time	Max	45	ns
			Read ES Access time(2)			
t_{WHBH}	t_R	Write Enable High to Ready/Busy High	Read Busy time	Max	60	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low		Max	100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		Min	80	ns
t_{VHWH}(3)	t_{WW}	Write Protection time		Min	100	ns
t_{VLWH}(3)				Min	100	ns

1. AC Characteristics for V_{DDQ} 1.8V devices are still to be determined.
2. ES = Electronic Signature.
3. $\overline{WP}$ High to $\overline{W}$ High during Program/Erase Enable operations.

Figure 13. Command Latch AC Waveforms

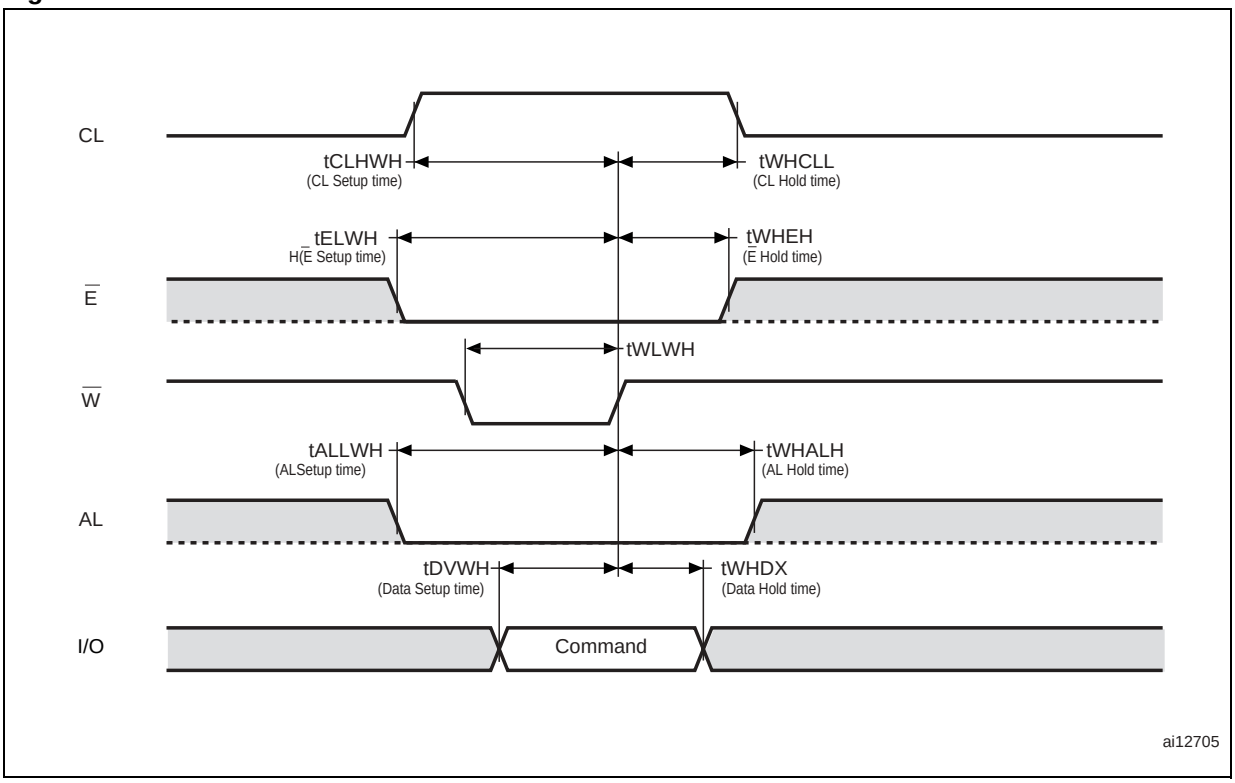


Figure 14. Address Latch AC Waveforms

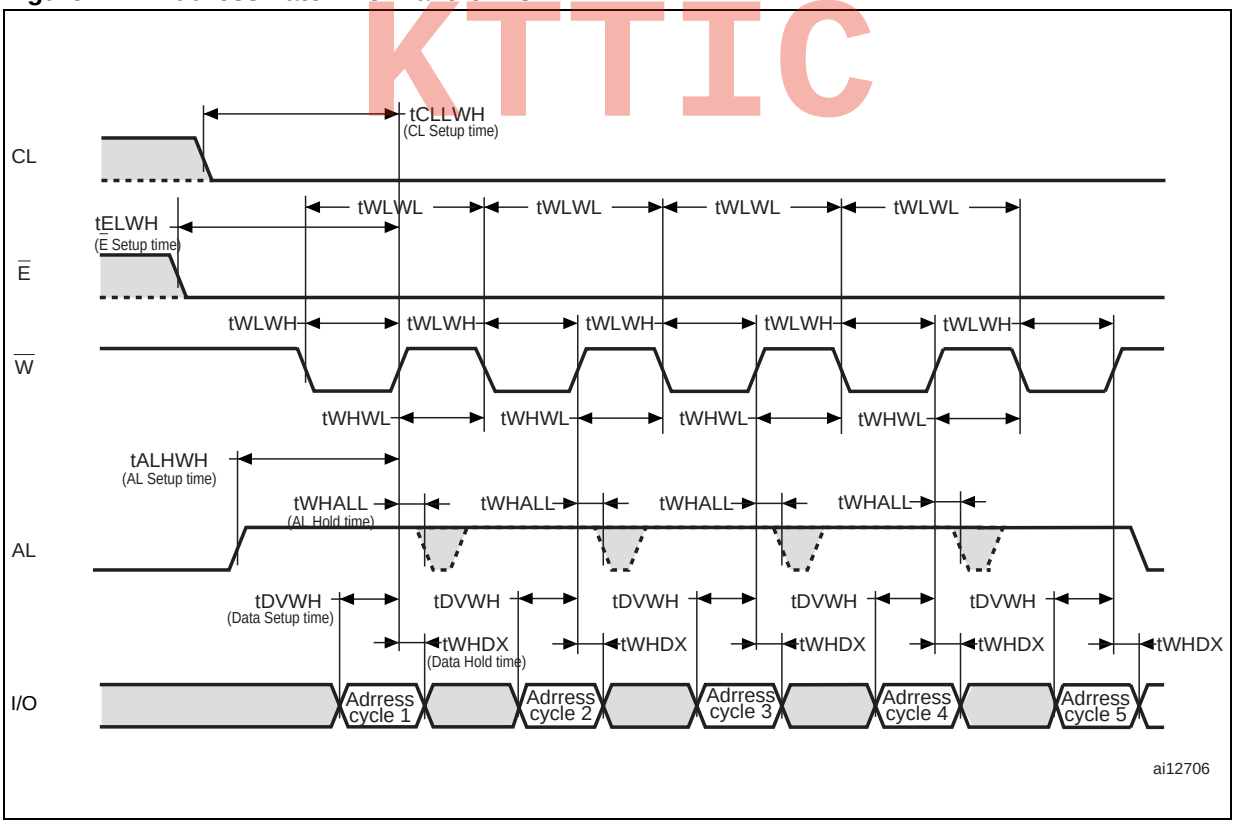
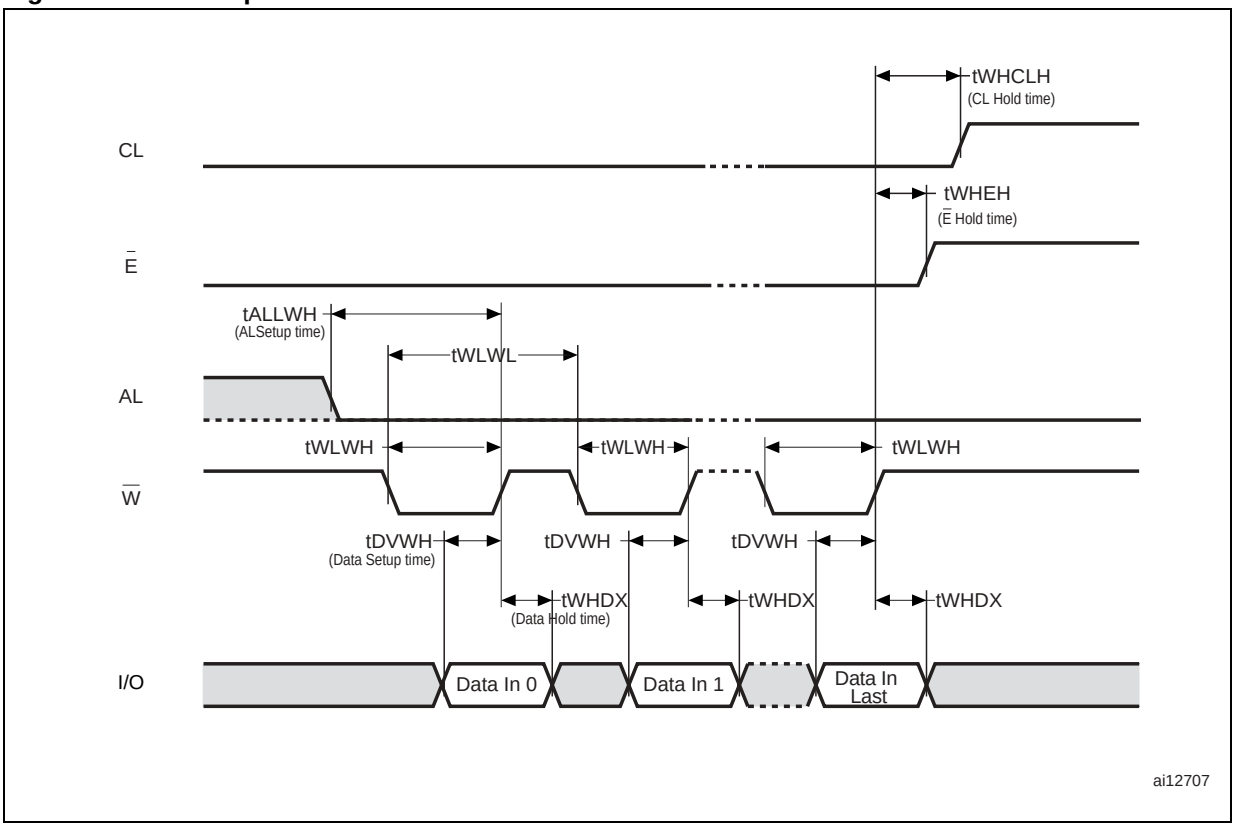
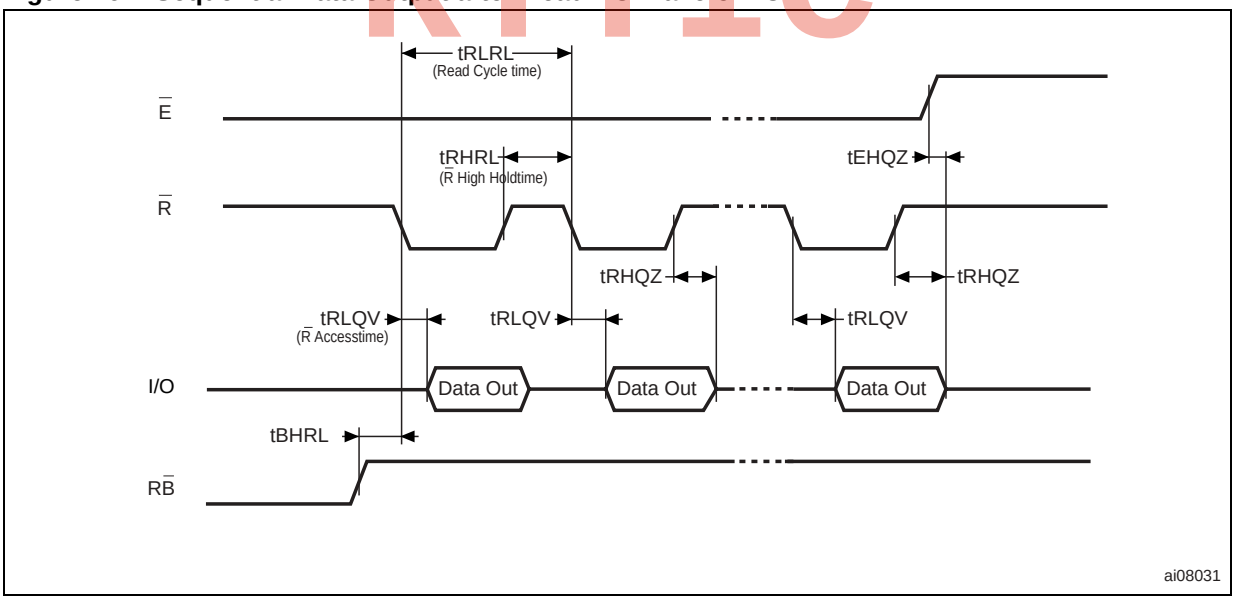


Figure 15. Data Input Latch AC Waveforms



1. Last Data In is 2111b.

Figure 16. Sequential Data Output after Read AC Waveforms



1. CL = Low, AL = Low, W = High.

Figure 17. Read Status Register AC Waveform

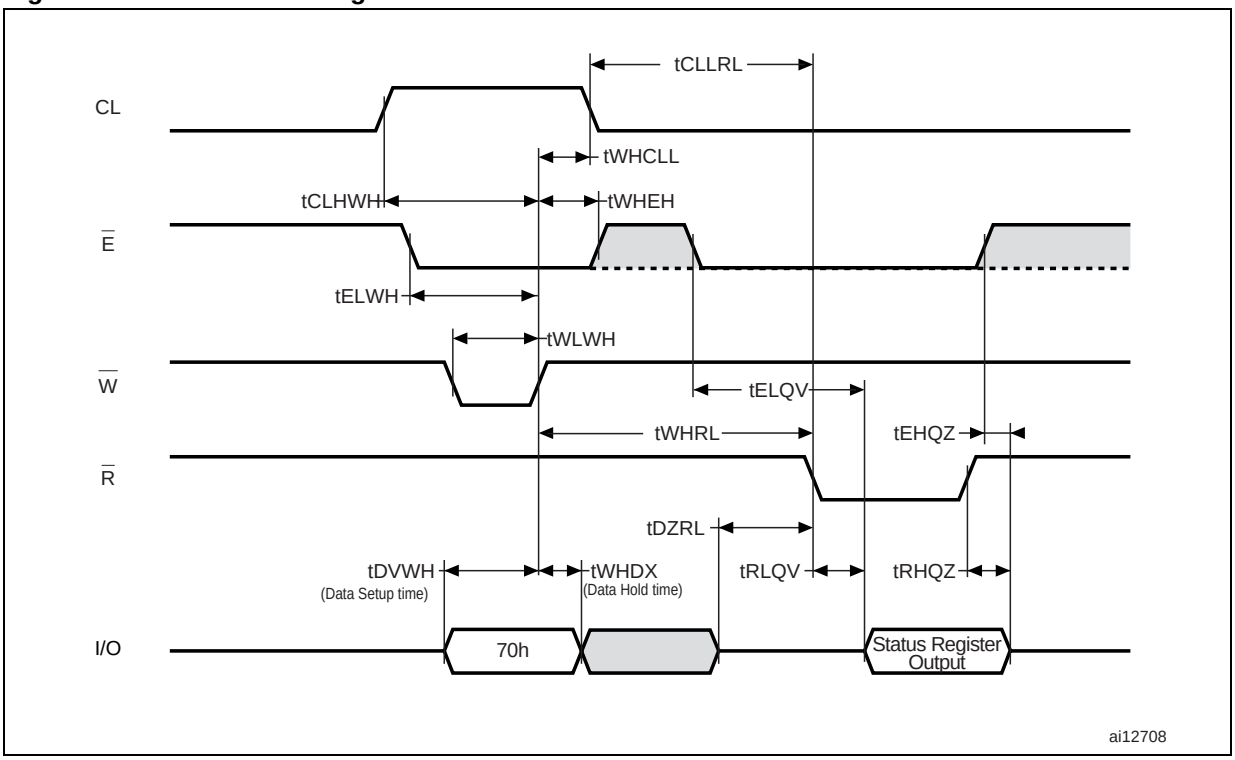
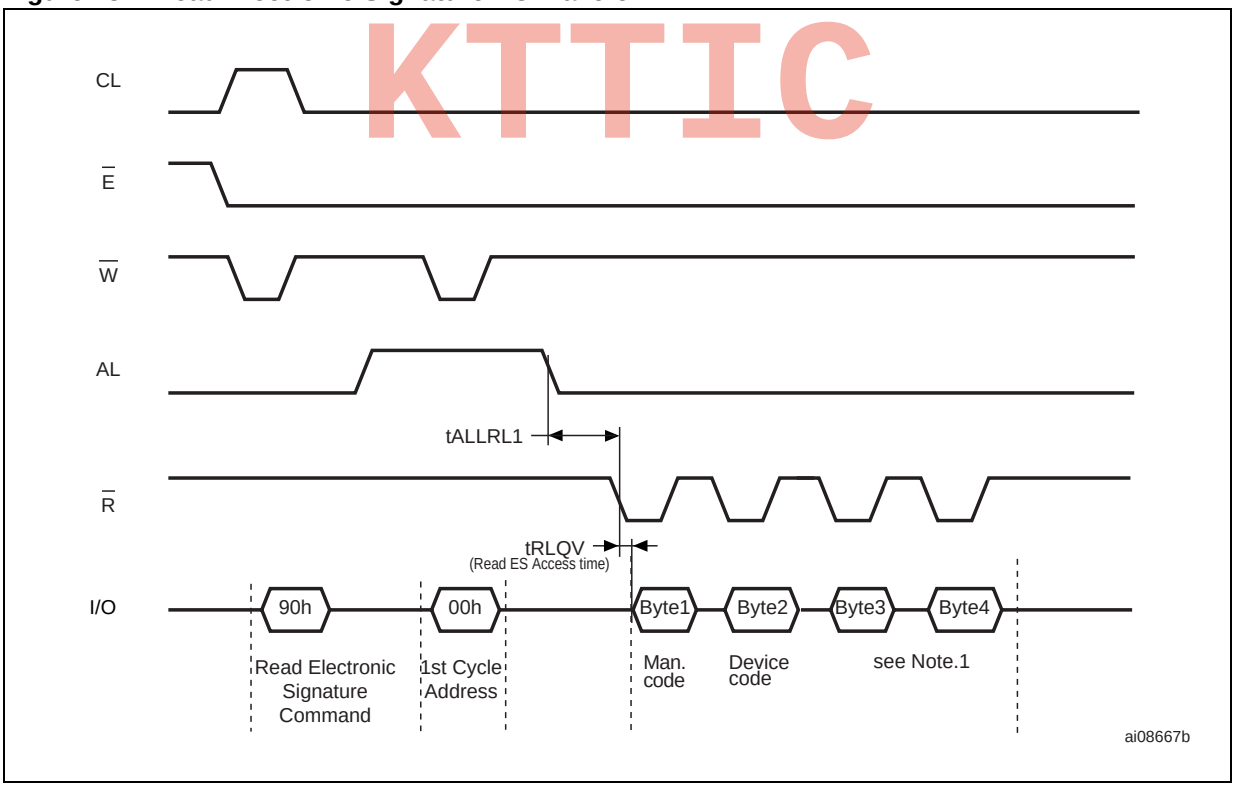


Figure 18. Read Electronic Signature AC Waveform



1. Refer to *Table 10* for the values of the Manufacturer and Device Codes, and to *Table 11* and *Table 12* for the information contained in Byte3 and Byte 4.

Figure 19. Page Read Operation AC Waveform

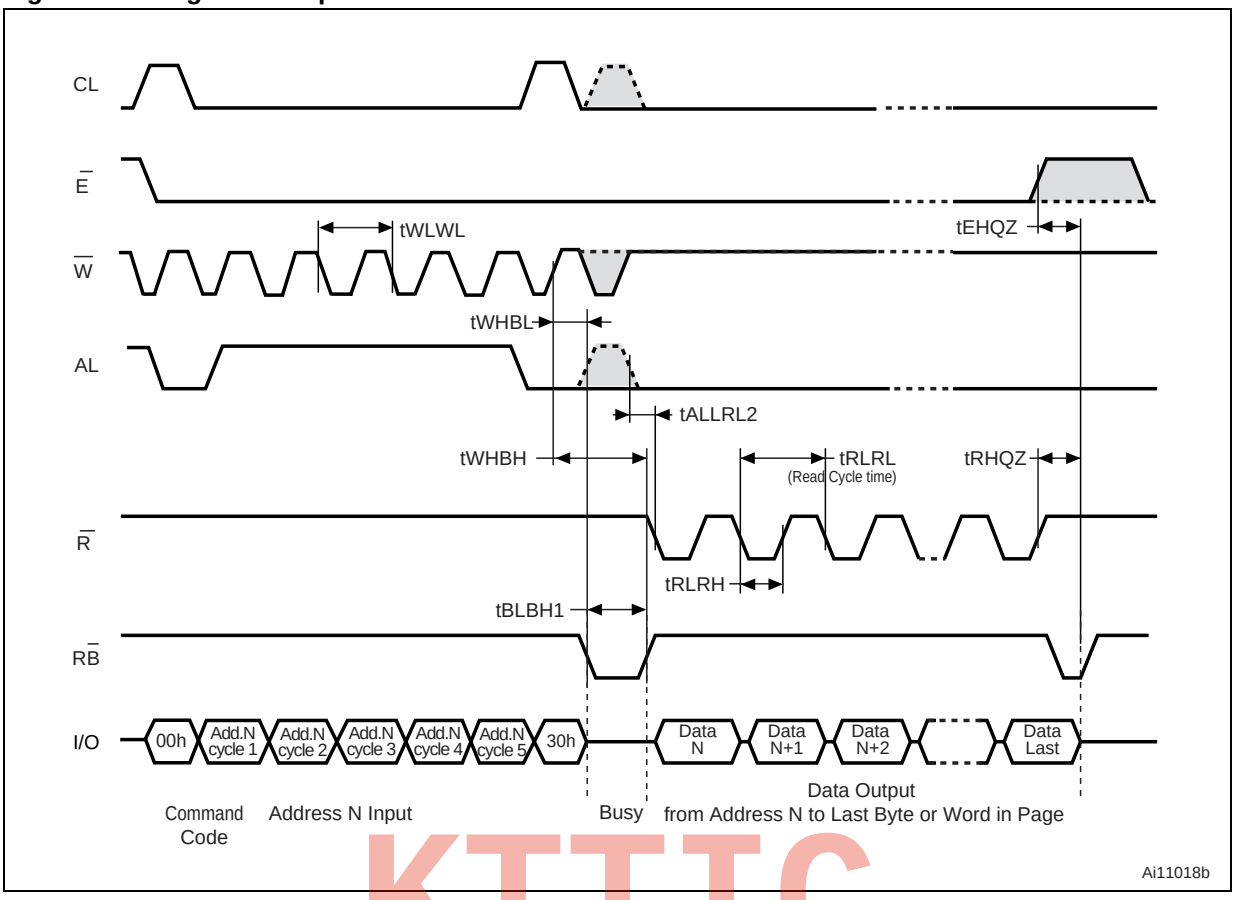


Figure 20. Page Program AC Waveform

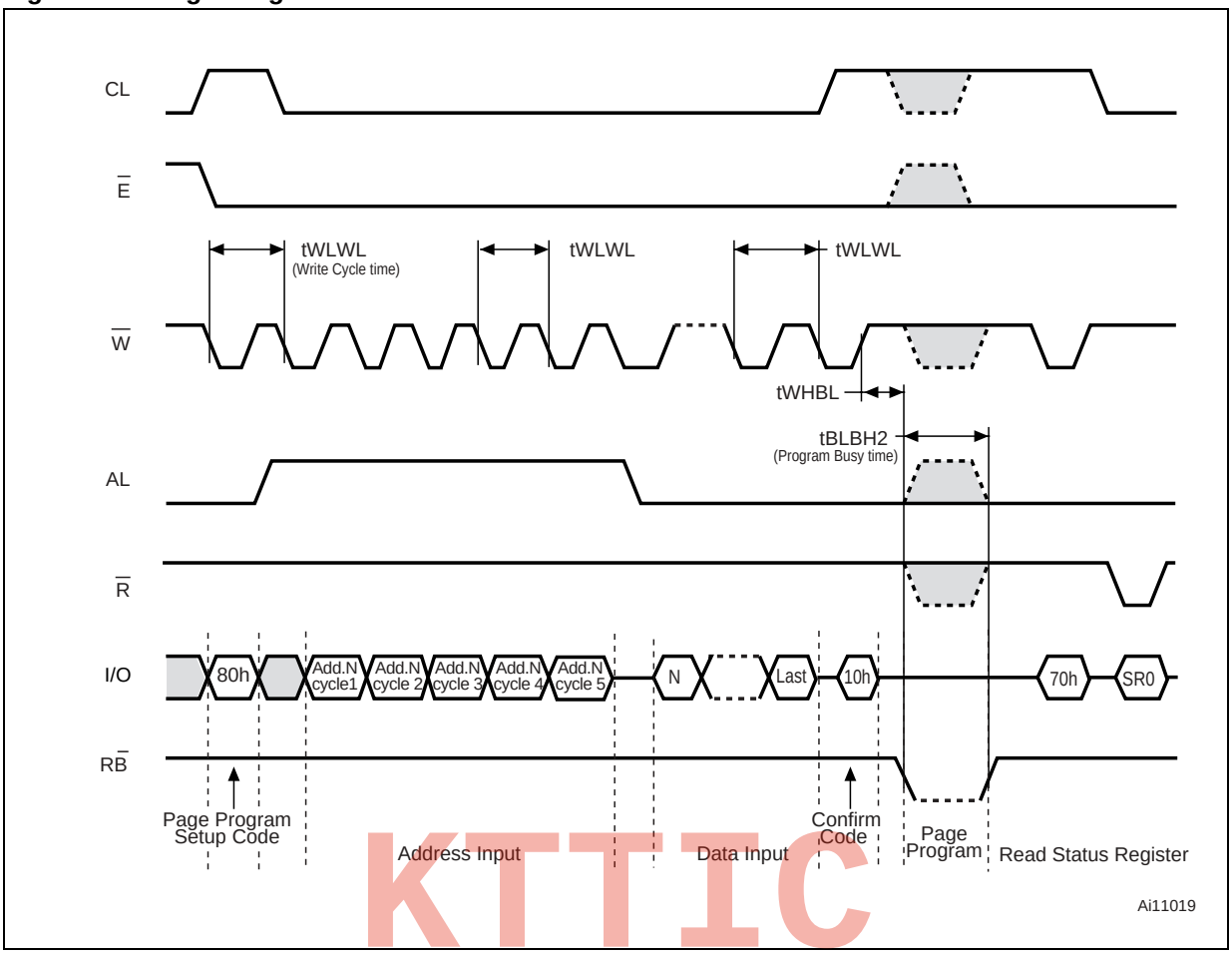


Figure 21. Block Erase AC Waveform

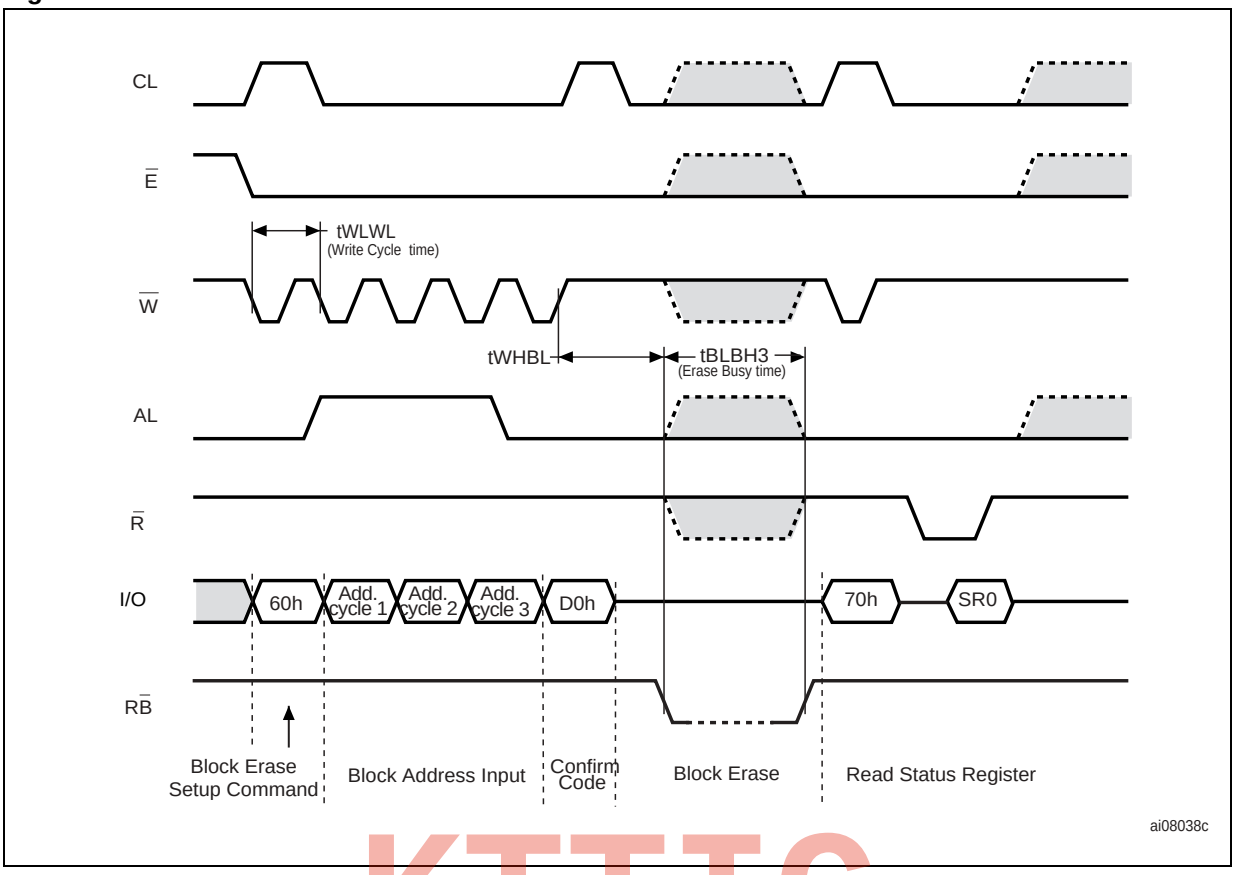


Figure 22. Reset AC Waveform

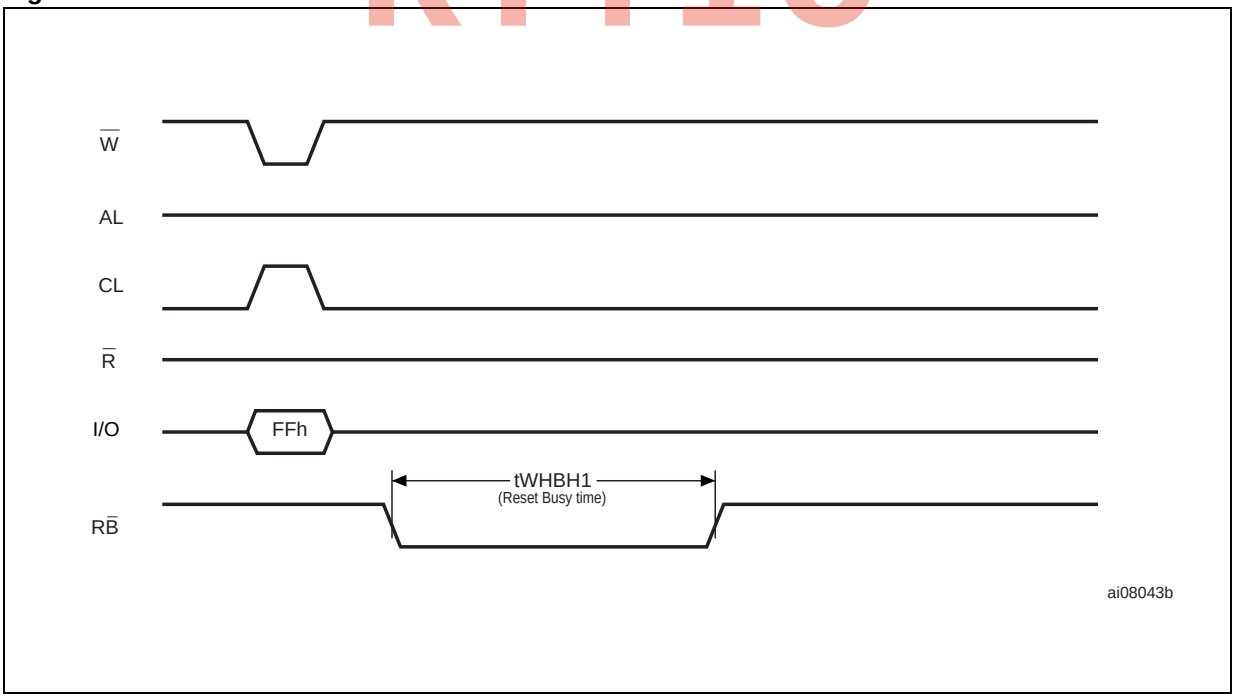


Figure 23. Program/Erase Enable Waveform

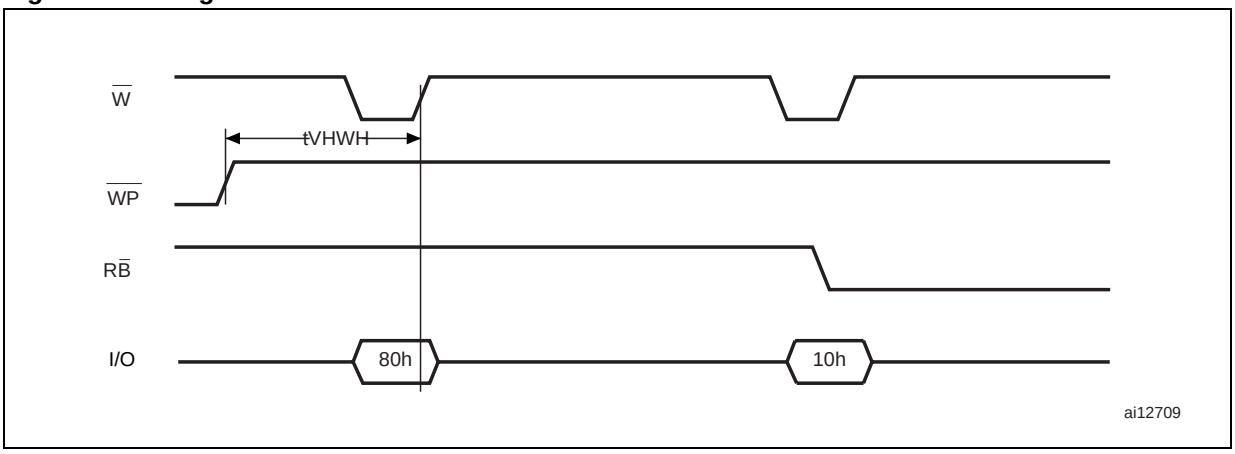
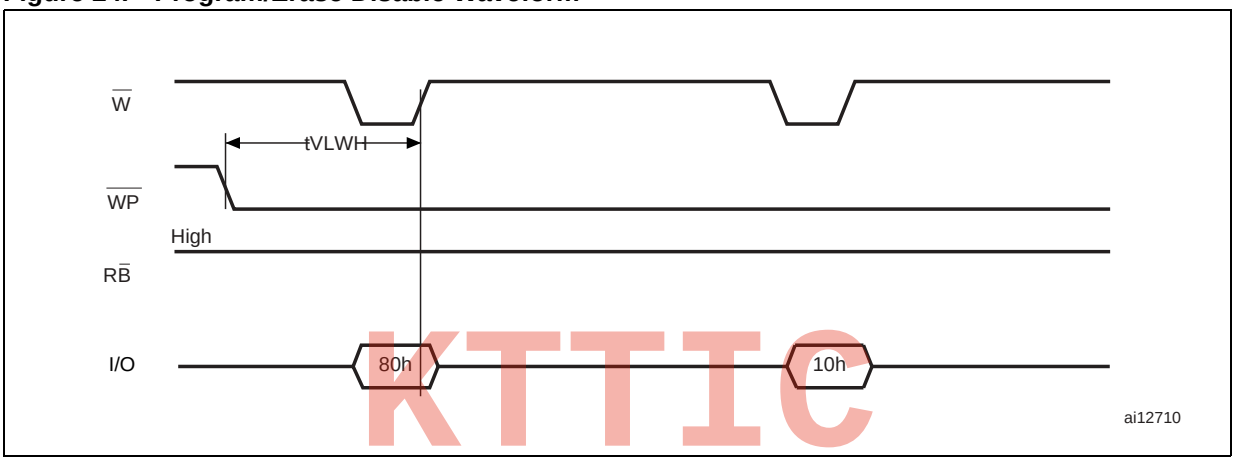


Figure 24. Program/Erase Disable Waveform



12.1 Ready/busy signal electrical characteristics

Figure 25, *Figure 26* and *Figure 27* show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + I_L}$$

So,

$$R_P min(1.8V) = \frac{1.85V}{3mA + I_L}$$

$$R_P min(3V) = \frac{3.2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 25. Ready/Busy AC Waveform

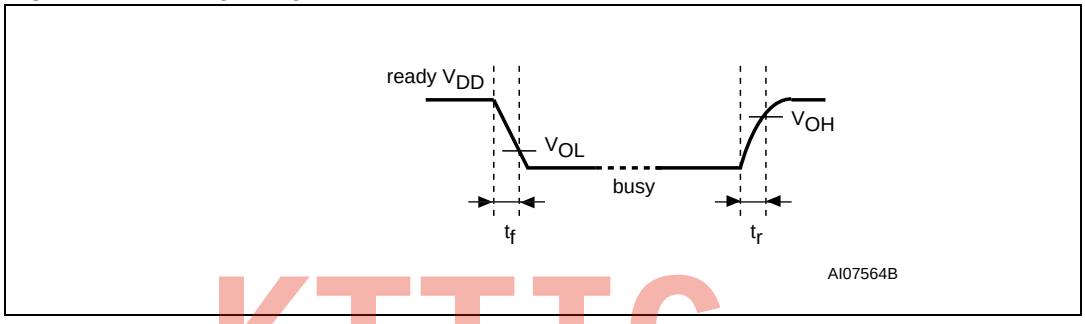


Figure 26. Ready/Busy Load Circuit

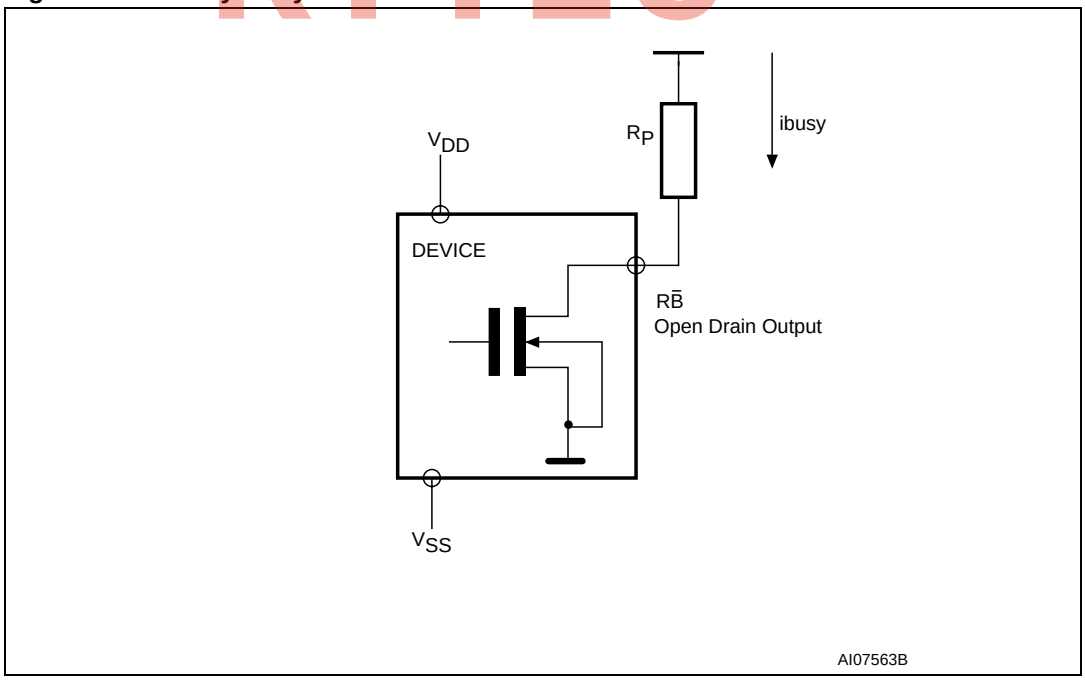
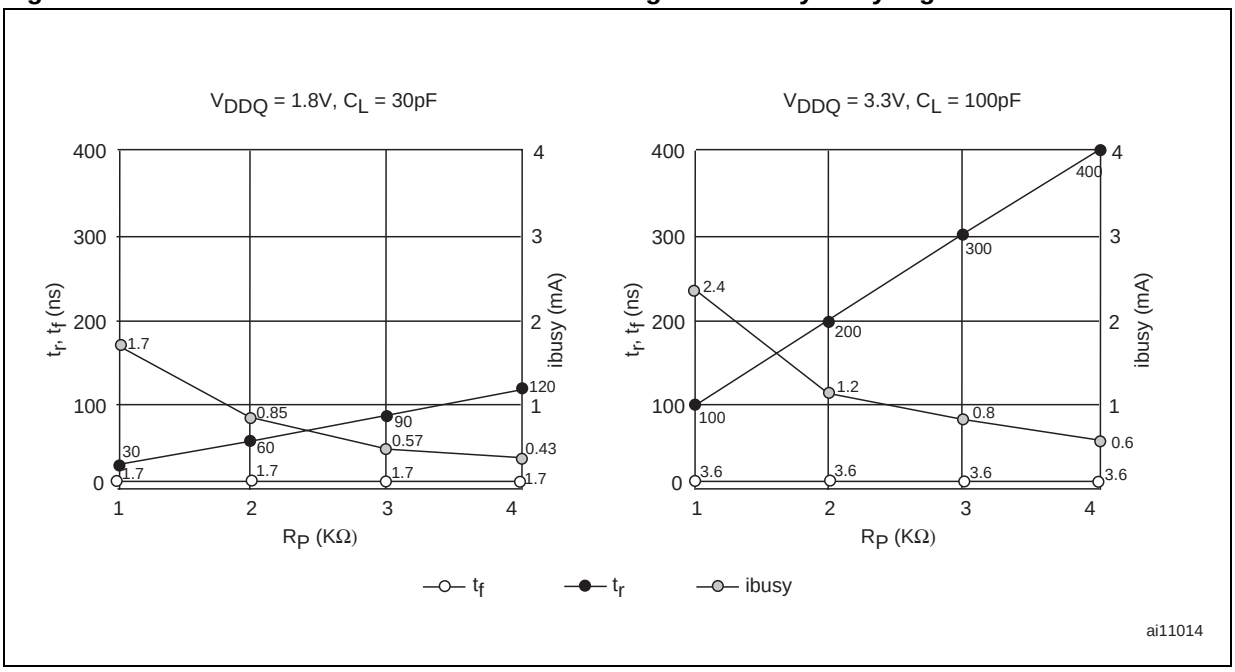


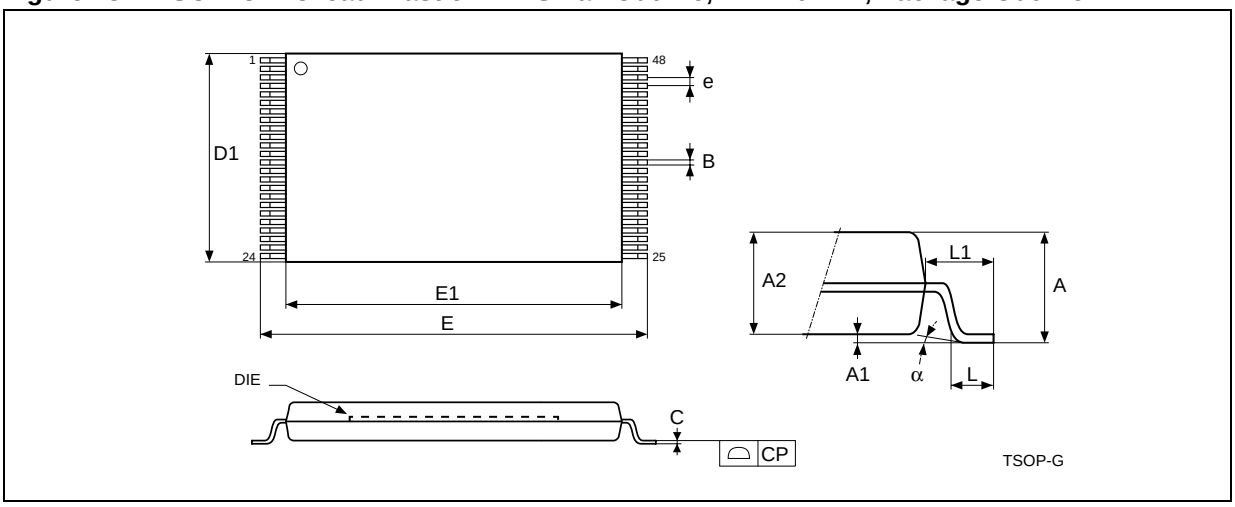
Figure 27. Resistor Value Versus Waveform Timings For Ready/Busy Signal



1. T = 25°C.

13 Package mechanical

Figure 28. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20 mm, Package Outline



1. Drawing is not to scale.

Table 21. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20 mm, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.100	0.050	0.150	0.0039	0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
B	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.080			0.0031
D1	12.000	11.900	12.100	0.4724	0.4685	0.4764
E	20.000	19.800	20.200	0.7874	0.7795	0.7953
E1	18.400	18.300	18.500	0.7244	0.7205	0.7283
e	0.500	–	–	0.0197	–	
L	0.600	0.500	0.700	0.0236	0.0197	0.0276
L1	0.800			0.0315		
a	3°	0°	5°	3°	0°	5°

14 Part numbering

Table 22. Ordering Information Scheme

Example: NAND04GW3C2A N 1 E

Device Type
NAND Flash Memory

Density
04G = 4Gb

Operating Voltage
W = V_{DDQ} = 2.7 to 3.6V
A = V_{DDQ} = 1.7V to 1.95V

Bus Width
3 = x8

Family Identifier
C = 2112 Bytes Page MLC

Device Options
2 = Chip Enable Don't Care Enabled

Product Version
A = First Version

Package
N = TSOP48 12 x 20mm (all devices)

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
E = ECOPACK Package, Standard Packing
F = ECOPACK Package, Tape & Reel Packing

Devices are shipped from the factory with the memory content bits, in valid blocks, erased to '1'. For further information on any aspect of this device, please contact your nearest ST Sales Office.

15 Revision history

Table 23. Document revision history

Date	Revision	Changes
16-Mar-2006	1	Initial release.
09-Nov-2006	2	NAND08GA2C2A and NAND08GW2C2A root part numbers removed.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com