



## EMIF08-LCD04M16

8-line L-C IPAD™, EMI filter and ESD protection in  $\mu$ QFN

### Features

- High cut off frequency low-pass filter:  
 $F_C = 400$  MHz at -6 dB
- High efficiency in EMI filtering:  
better than -35 dB from 900 MHz to 2 GHz
- Very low PCB space consuming with plastic micro-package 1.35 x 1.7 mm
- Very thin package: 0.55 mm
- High efficiency in ESD (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration
- ECOPACK®2 compliant component

### Complies with the following standards

- IEC61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

### Application

Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for mobile phones
- Computers and printers
- Communication systems
- MCU Boards

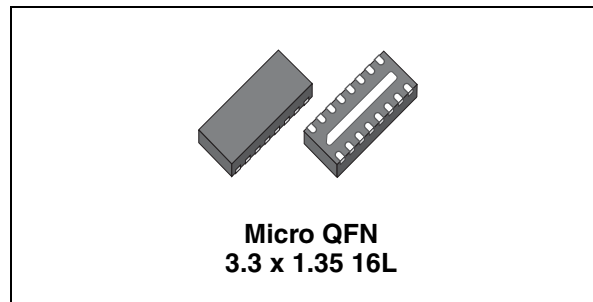
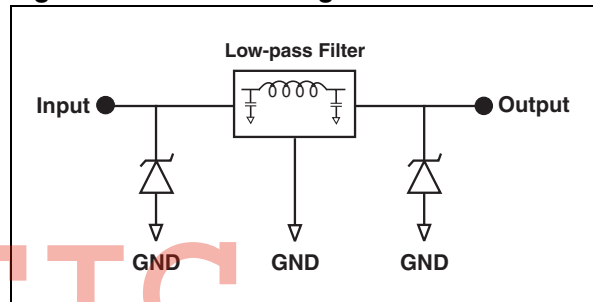


Figure 1. Device configuration



### Description

The EMIF08-LCD04M16 is a 8-line inductor-capacitor (LC) EMI filter designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences requiring a large bandwidth.

This filter includes an ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV contact discharge.

TM: IPAD is a trademark of STMicroelectronics.

# 1 Electrical characteristics

**Table 1. Absolute maximum ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter	Value	Unit
$V_{PP}$	ESD discharge IEC61000-4-2, contact discharge	$\pm 15$	kV
$T_{op}$	Operating temperature range	-40 to 85	$^{\circ}\text{C}$
$T_j$	Maximum junction temperature	125	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

**Table 2. Electrical characteristics ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameters								
$V_{BR}$	Breakdown voltage								
$I_{RM}$	Leakage current @ $V_{RM}$								
$V_{RM}$	Stand-off voltage								
$V_{CL}$	Clamping voltage								
$V_F$	Forward voltage								
$R_d$	Dynamic impedance								
$I_{PP}$	Peak pulse current								
$R_{I/O}$	Series resistance between input and output								
$C_{line}$	Input capacitance per line								
$F_C$	Cut-off Frequency								
Symbol	Test conditions					Min.	Typ.	Max.	Unit
$V_{BR}$	$I_R = 1\text{ mA}$					6	-	-	V
$I_{RM}$	$V_{RM} = 3\text{ V per line}$	-	-	100	nA				
L	Inductance	-	12	-	nH				
$C_{line}$	$V_R = 3\text{ V DC}$ , $F = 1\text{ MHz}$ , $V_{osc} = 30\text{ mV}$	17	18	19	pF				
R	Parasitic resistance of the inductance	9	12.5	20	$\Omega$				
$F_C$	50 $\Omega$ source and 50 $\Omega$ load termination at -6 dB	-	400	-	MHz				

Figure 2. S21 attenuation measurements

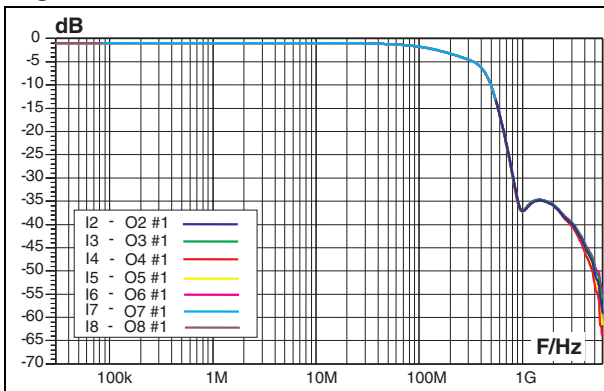


Figure 3. Analog crosstalk measurements

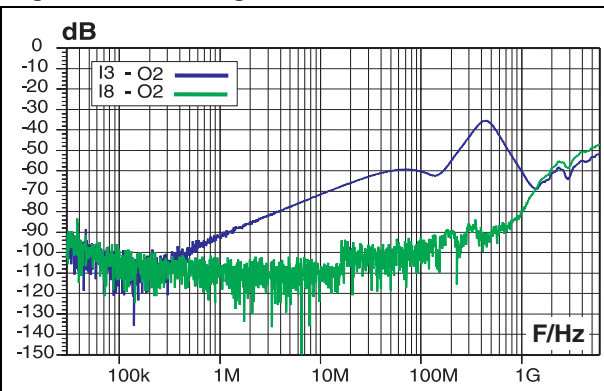


Figure 4. ESD response to IEC61000-4-2 (+15 kV air discharge)

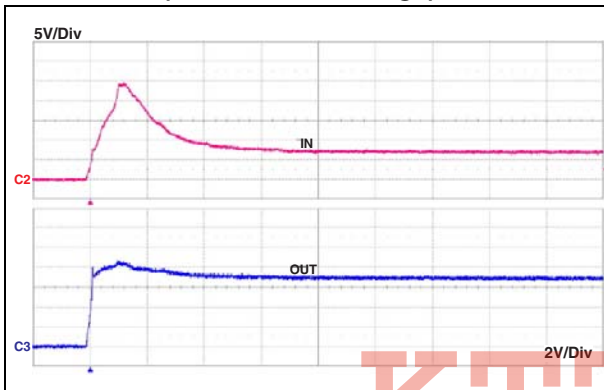


Figure 5. ESD response to IEC61000-4-2 (-15 kV air discharge)

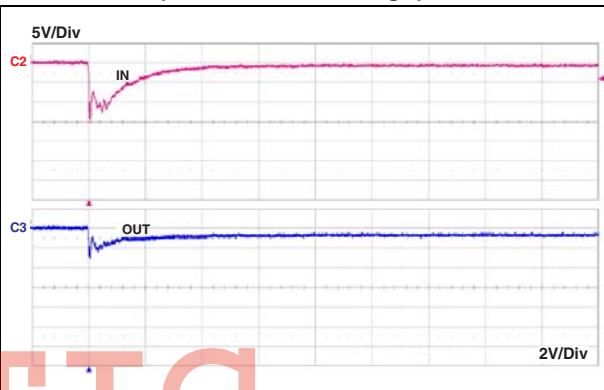
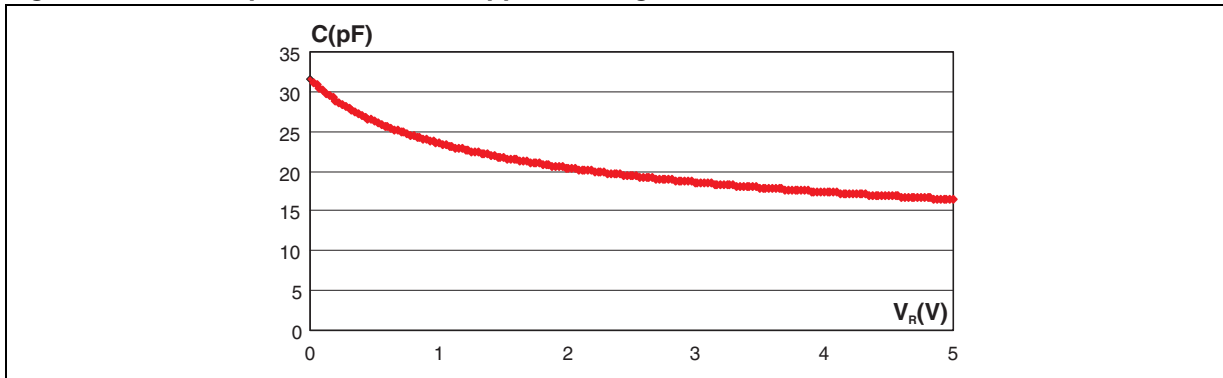
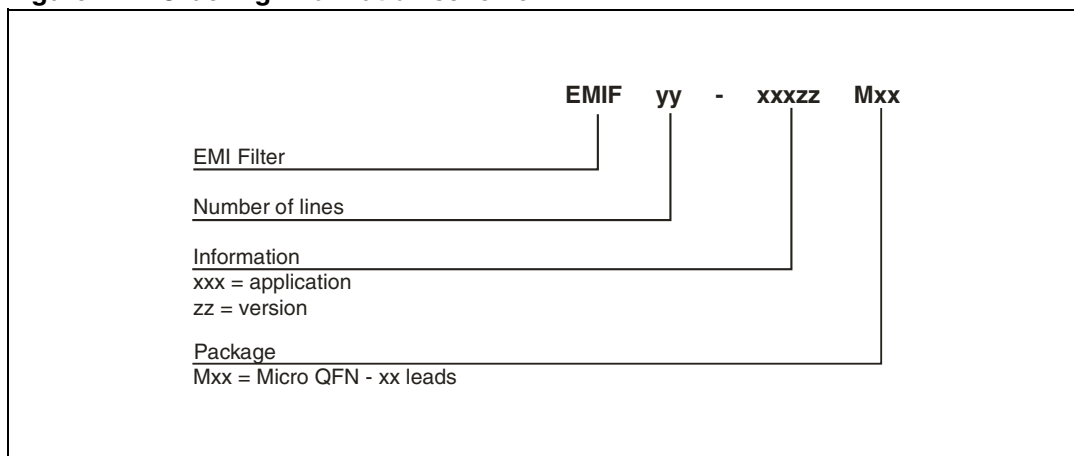


Figure 6. Line capacitance versus applied voltage



## 2 Ordering information scheme

Figure 7. Ordering information scheme



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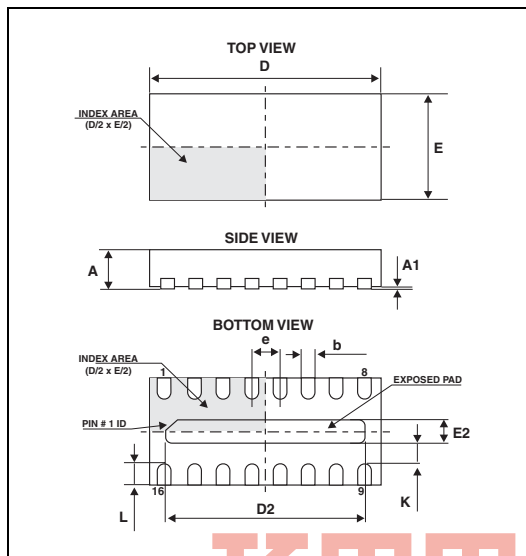
### 3 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

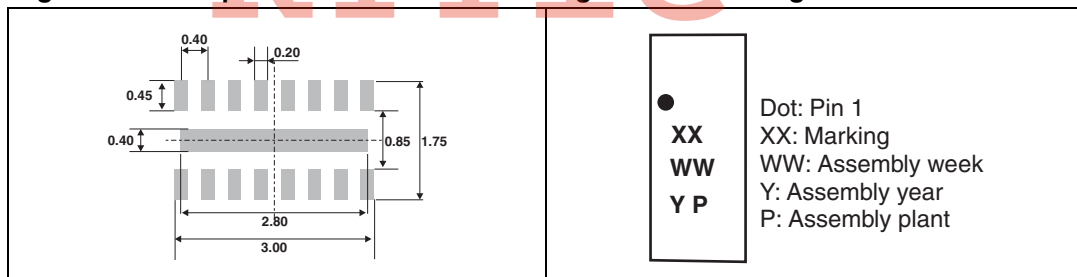
**Table 3. Micro QFN 3.3x1.35 16L dimensions**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.00	0.0008	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	-	3.30	-	-	0.13	-
D2	2.65	2.80	2.90	0.104	0.110	0.114
E	-	1.35	-	-	0.053	-
E2	0.25	0.40	0.50	0.010	0.016	0.020
e	-	0.40	-	-	0.016	-
k	0.20	-	-	0.008	-	-
L	0.15	0.25	0.35	0.006	0.010	0.014



**Figure 8. Footprint**

**Figure 9. Marking**



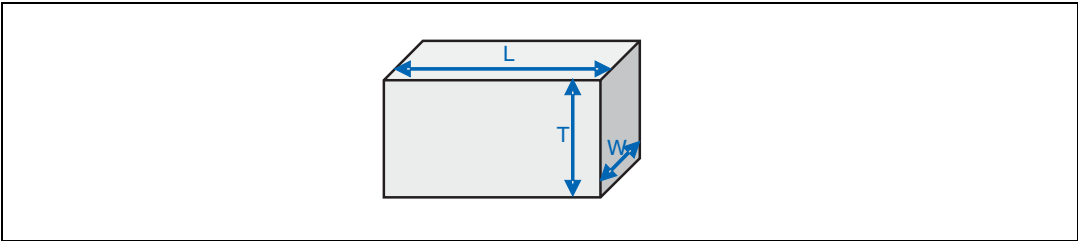
*Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.*

## 4 Recommendation on PCB assembly

### 4.1 Stencil opening design

1. General recommendation on stencil opening design
  - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

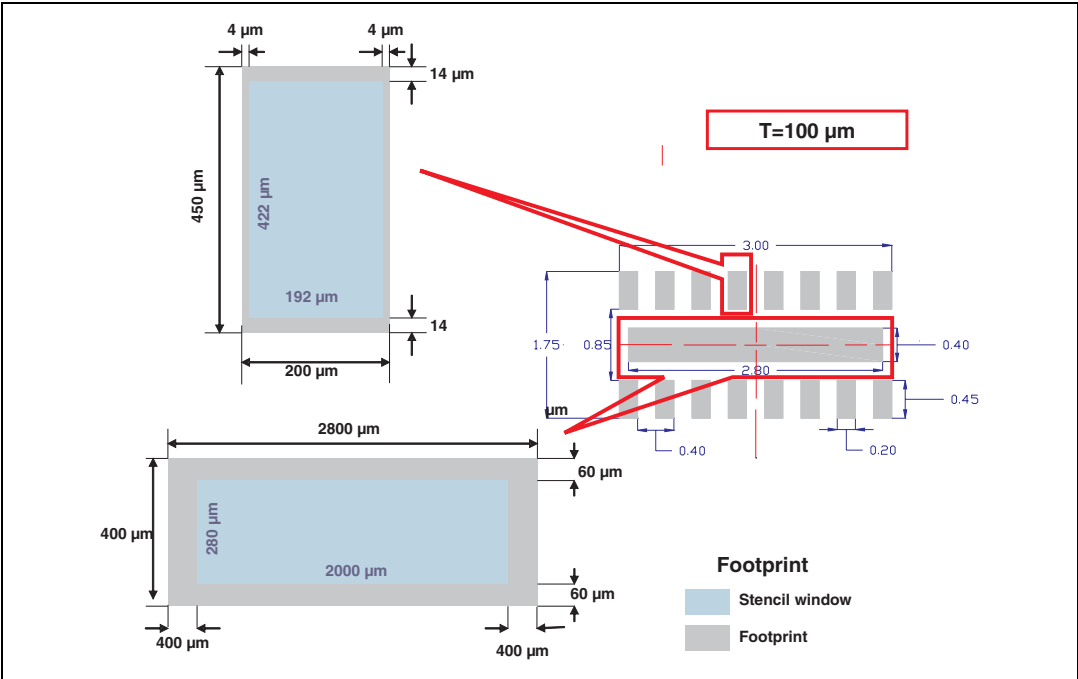
Figure 10. Stencil opening dimensions



- b) General design rule
  - Stencil thickness (T) = 75 ~ 125 μm
  - Aspect Ratio =  $\frac{W}{T} \geq 1.5$
  - Aspect Area =  $\frac{L \times W}{2T(L + W)} \geq 0.66$

2. Reference design
  - a) Stencil opening thickness: 100 μm
  - b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
  - c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 11. Recommended stencil window position



## 4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45  $\mu\text{m}$ .

## 4.3 Placement

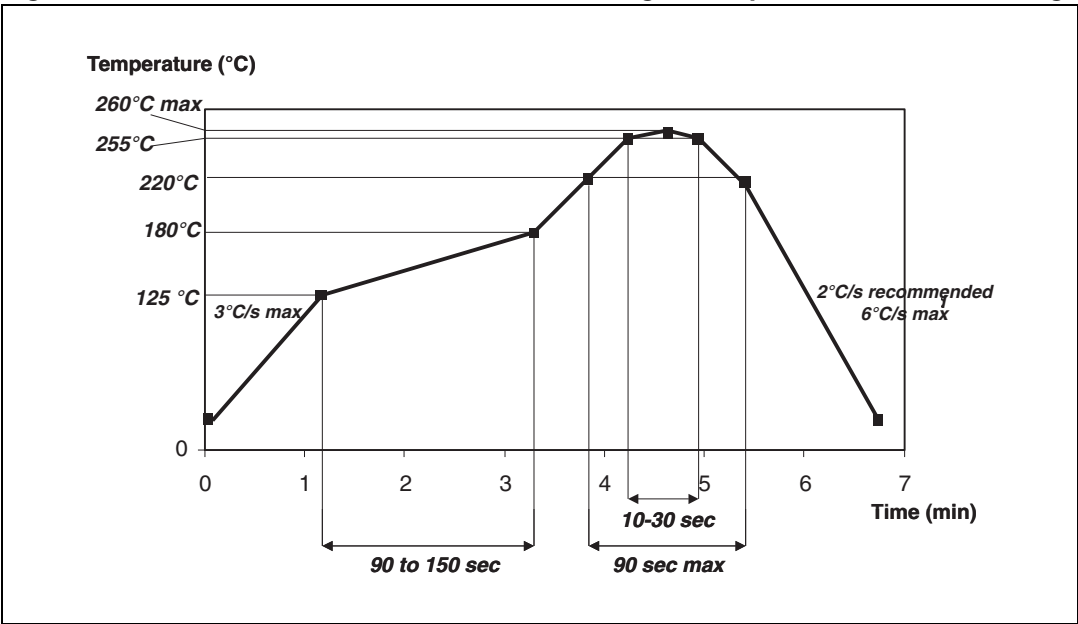
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of  $\pm 0.05$  mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

## 4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

### 4.5 Reflow profile

Figure 12. ST ECOPACK<sup>®</sup> recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.





## 5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF08-LCD04M16	JA <sup>(1)</sup>	μQFN	6.74 mg	3000	Tape and reel

1. The marking can be rotated by 90° to differentiate assembly location

## 6 Revision history

Table 5. Document revision history

Date	Revision	Changes
20-May-2009	1	Initial release.

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