EMIF03-SIM02C2

IPAD™

3 line EMI filter including ESD protection

Main product characteristics

Where EMI filtering in ESD sensitive equipment is required:

- SIM Interface (Subscriber Identify Module)
- UIM Interface (Universal Identify Module)

Description

The EMIF03-SIM02C2 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The EMIF03 Flip-Chip packaging means the package size is equal to the die size.

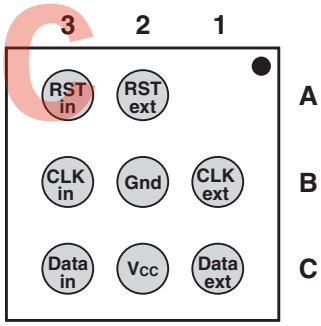
This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.

Benefits

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead free coated package
- Very low PCB space consuming:
  - 1.42mm x 1.42mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging

Coated Flip-Chip package (8 bumps)

Pin configuration (Bump side)



Complies with following standards:

IEC 61000-4-2

Level 4 on external and V_{CC} pins:

15 kV (air discharge)

8 kV (contact discharge

Level 1 on internal pins:

2 kV (air discharge)

2 kV (contact discharge

MIL STD 883G - Method 3015-7 Class 3

1 Characteristics

Figure 1. Basic cell configuration

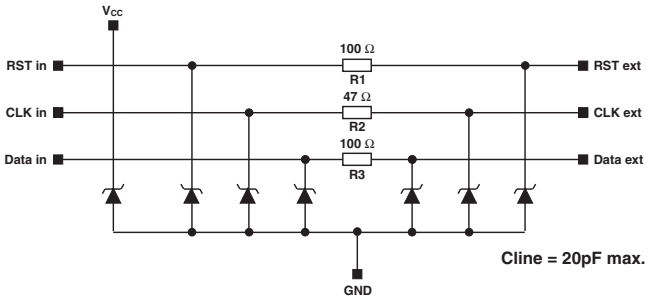
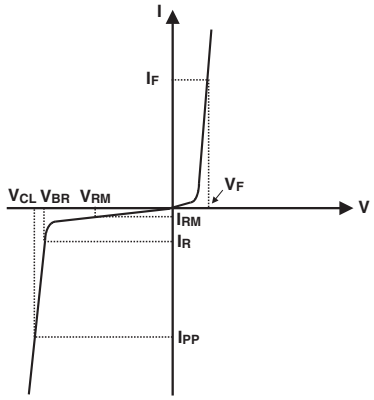


Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
V_{PP}	**Internal pins (A3, B3, C3):** ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge **External pins (A2, B1, C2, C1):** ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	 2 2 15 8	kV
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Table 2. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between input and output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	I_R = 1 mA	6		20	V
I_{RM}	V_{RM} = 3 V			0.2	µA
R_d			1.5		Ω
R_1, R_3	Tolerance ± 20%		100		
R_2	Tolerance ± 20%		47		
C_{line}	V_R = 0 V			20	pF

Figure 2. S21 (dB) attenuation measurement (A2-A3 line)

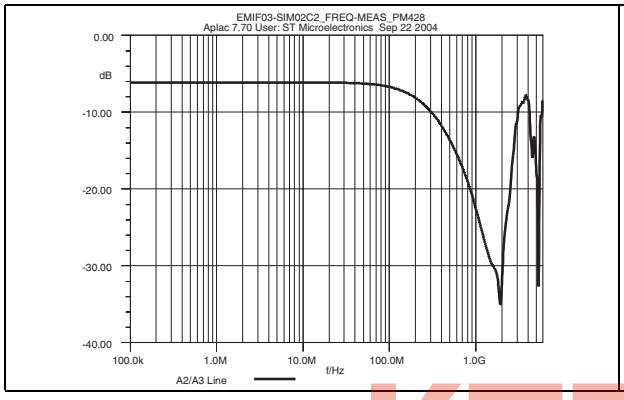


Figure 3. S21 (dB) attenuation measurement (B1-B3 line)

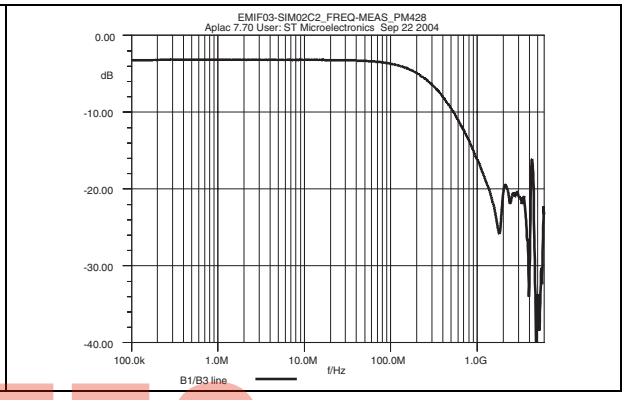


Figure 4. S21 (dB) attenuation measurement (C1-C3 line)

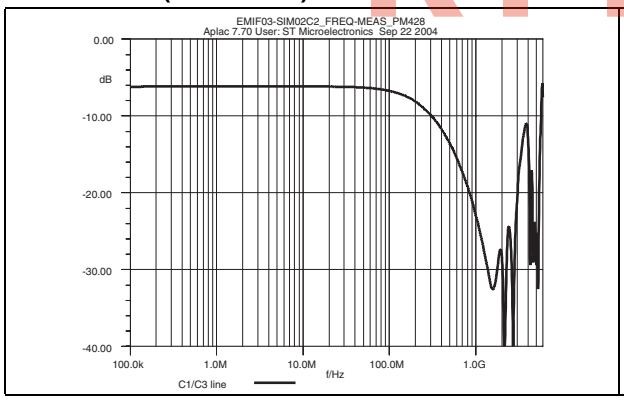


Figure 5. Analog crosstalk measurements

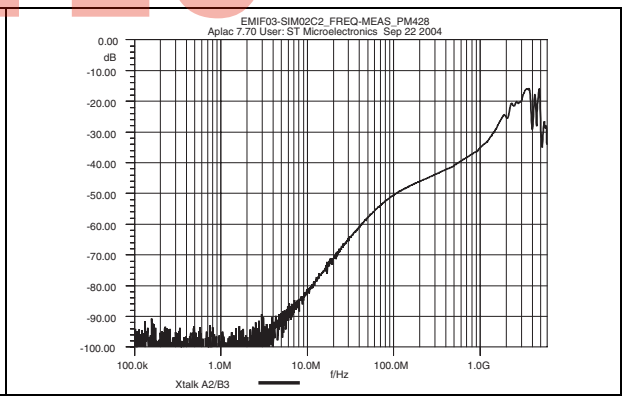


Figure 6. Voltages when IEC 61000-4-2 (+15 kV air discharge) applied to external pin

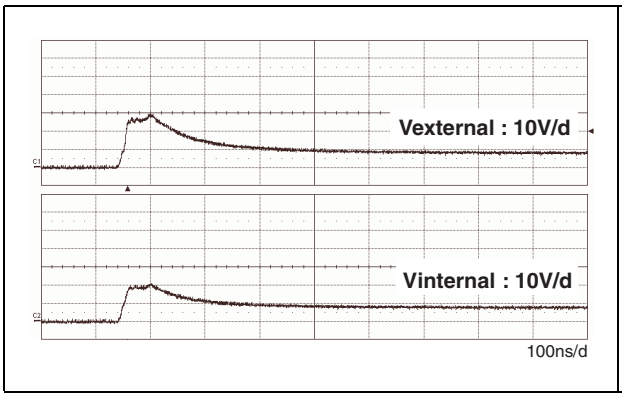


Figure 7. Voltages when IEC 61000-4-2 (-15 kV air discharge) applied to external pin

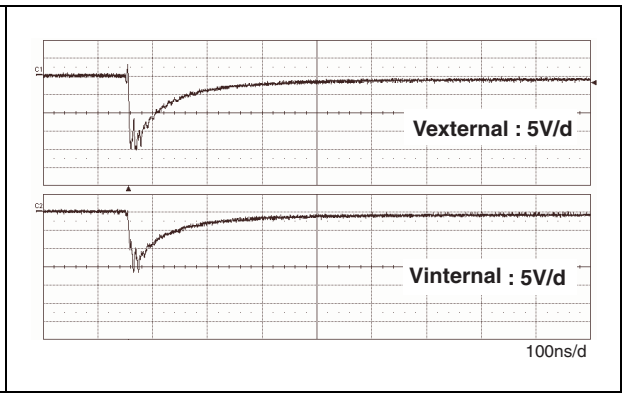


Figure 8. Line capacitance versus reverse applied voltage (typical)

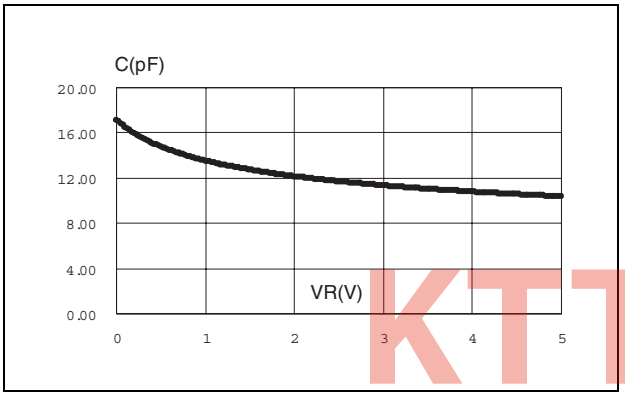


Figure 9. Aplac model

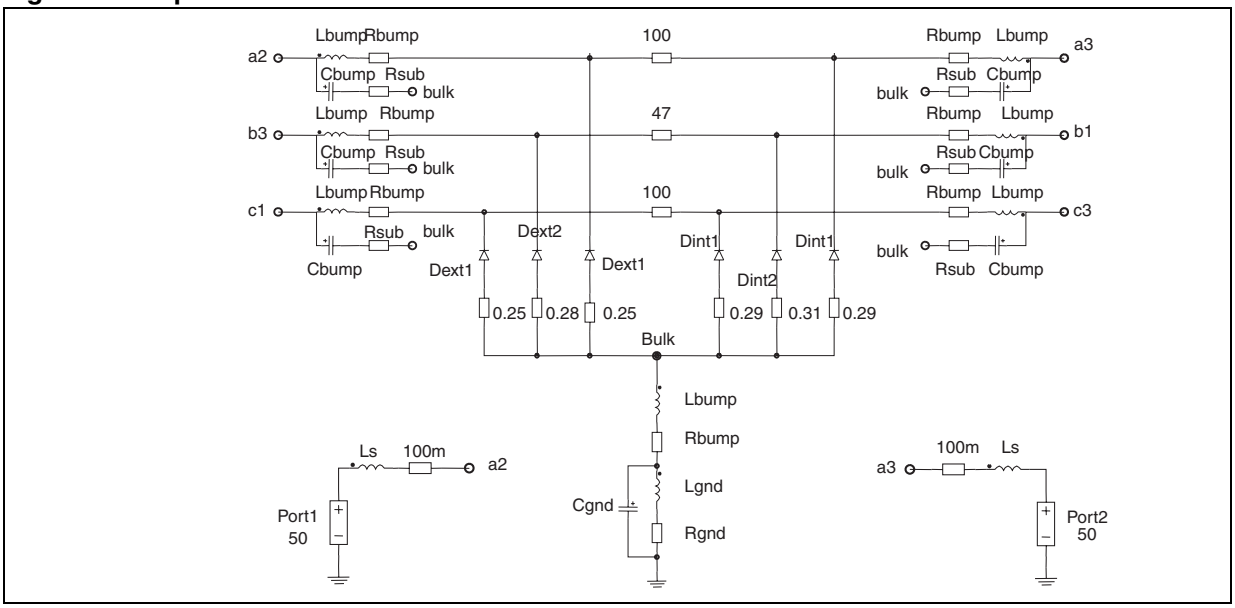
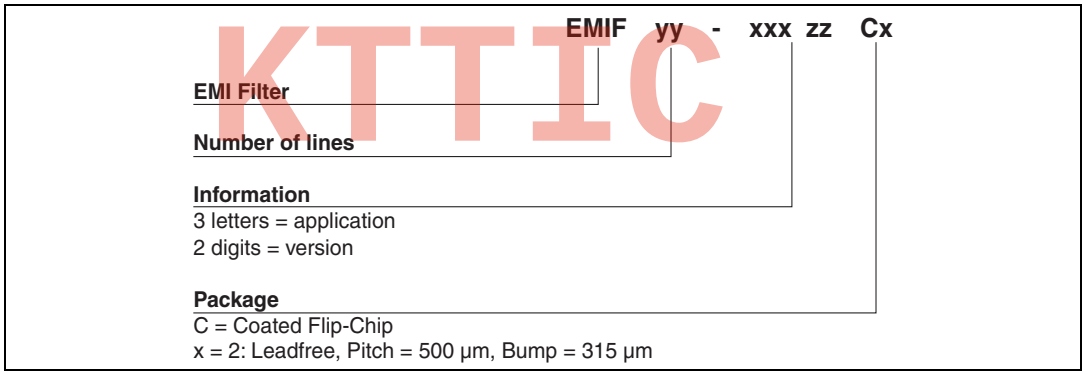


Figure 10. Aplac parameters

Ls 950pH				
Rs 150m	Model Dint1	Model Dext1	Model Dint2	Model Dext2
Cext1 15pF	BV=15	BV=15	BV=15	BV=15
Cint1 4.5pF	CJO=Cint1	CJO=Cext1	CJO=Cint2	CJO=Cext2
Cext2 14pF	IBV=1u	IBV=1u	IBV=1u	IBV=1u
Cint2 4pF	IKF=1000	IKF=1000	IKF=1000	IKF=1000
Rbump 20m	IS=10f	IS=10f	IS=10f	IS=10f
Lbump 50pH	ISR=100p	ISR=100p	ISR=100p	ISR=100p
Cbump 0.15pF	N=1	N=1	N=1	N=1
Rgnd 500m	M=0.3333	M=0.3333	M=0.3333	M=0.3333
Lgnd 50pH	RS=0.001m	RS=0.001m	RS=0.001m	RS=0.001m
Cgnd 0.15pF	VJ=0.6	VJ=0.6	VJ=0.6	VJ=0.6
Rsub 100m	TT=50n	TT=50n	TT=50n	TT=50n

2 Ordering information scheme



3 Package information

- Epoxy meets UL94, V0

Figure 11. Flip-Chip Dimensions

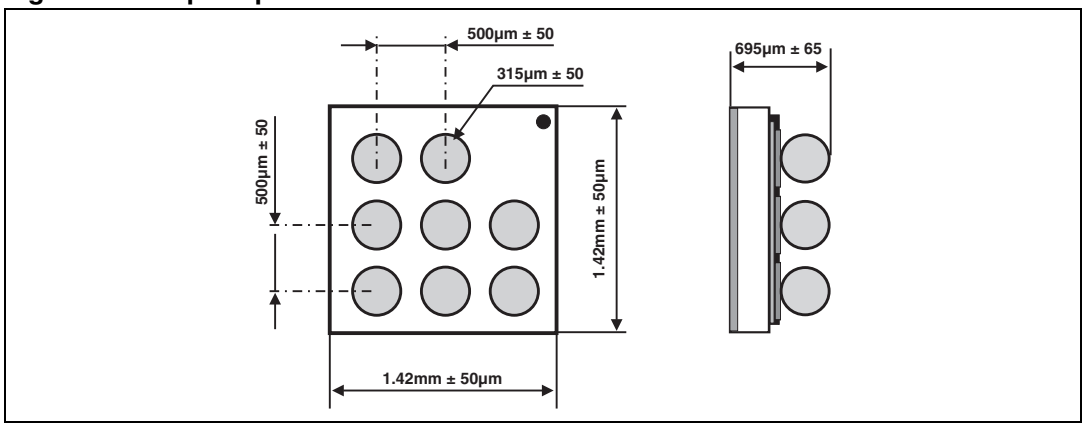


Figure 12. Marking

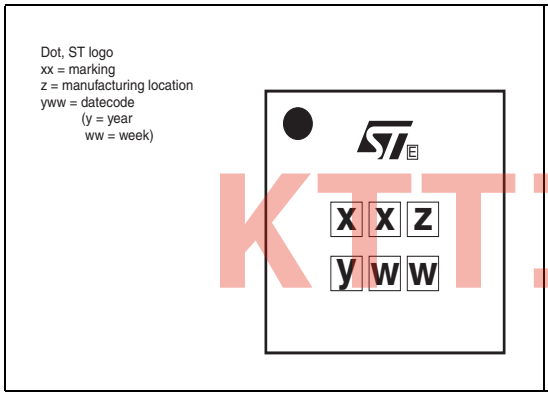


Figure 13. Footprint recommendation

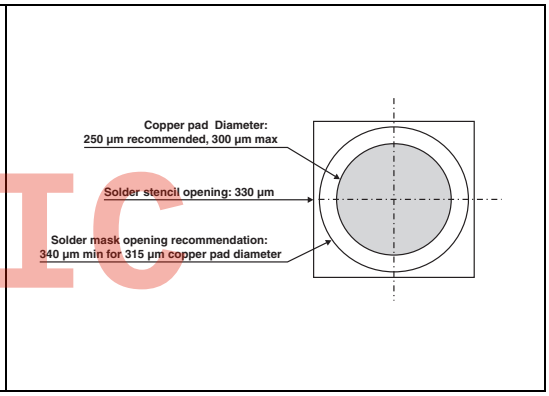
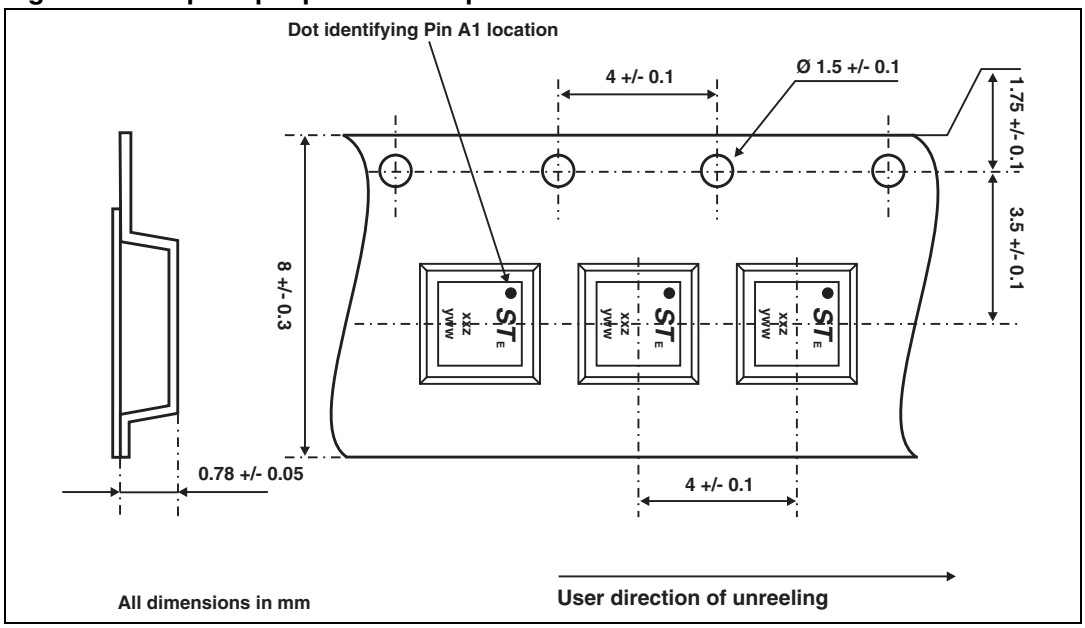


Figure 14. Flip-Chip tape and reel specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF03-SIM02C2	GJ	Flip-Chip	3.04 mg	5000	7” Tape and reel

5 Revision history

Date	Revision	Changes
07-Feb-2007	1	Initial release.
21-Mar-2007	2	Updated weight in Ordering information.

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