EMIF02-USB03F2

2-line IPAD™, EMI filter including ESD protection

Features

- 2-line low-pass-filter + 2-line ESD protection
- High efficiency in EMI filtering
- Lead-free package
- Very low PCB space occupation: < 3.25 mm²
- Very thin package: 0.65 mm
- High efficiency in ESD suppression (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reduction of parasitic elements through
- integration and wafer level packaging

Complies with the following standards

- IEC 61000-4-2 level 4 on external pins:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-2 level 1 on internal pins:
  - 2 kV (air discharge)
  - 2 kV (contact discharge)

Application

ESD protection and EMI filtering for:

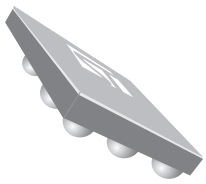
- USB OTG port

Description

The EMIF02-USB03F2 is a highly integrated array designed to suppress EMI / RFI noise for USB OTG (on-the-go).

The EMIF02-USB03F2 Flip Chip packaging means the package size is equal to the die size.

Additionally, this filter includes ESD protection circuitry which prevents damage to the protected device when subjected to ESD surges up to 15 kV on external contacts.



Flip Chip
(11 bumps)

Figure 1. Pin layout (bump side)

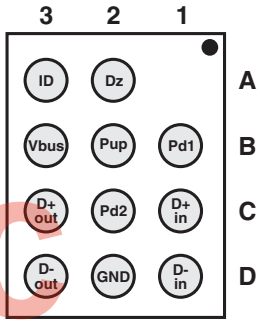
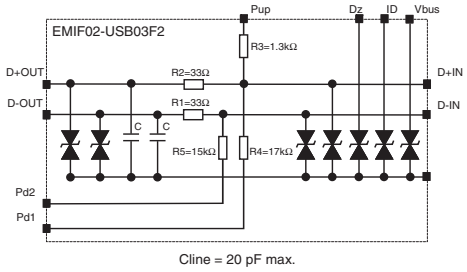


Figure 2. Schematic



TM: IPAD is a trademark of STMicroelectronics.

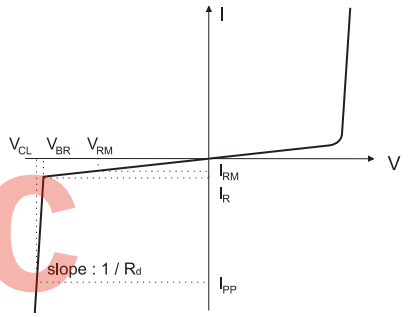
1 Characteristics

Table 1. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	**Internal pins (D3, C3, C2, B2, B1):** ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge **External pins (D1, C1, A2, A3, B3):** ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	 2 2 15 8	kV
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
C_{line}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	I_R = 1 mA	14			V
I_{RM}	V_{RM} = 3 V		0.1	0.5	µA
C_{line}	@ 0 V			20	pF
R_1, R_2	Tolerance ± 5 %		33		Ω
R_3	Tolerance ± 5 %		1.30		kΩ
R_4	Tolerance ± 5 %		17		kΩ
R_5	Tolerance ± 5 %		15		kΩ

Figure 3. Filtering measurement

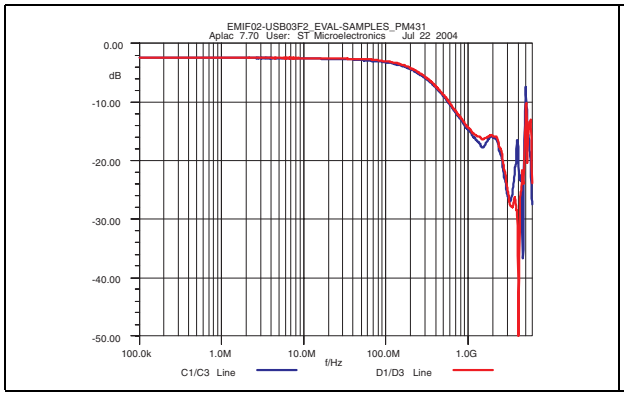


Figure 4. Analog crosstalk measurement

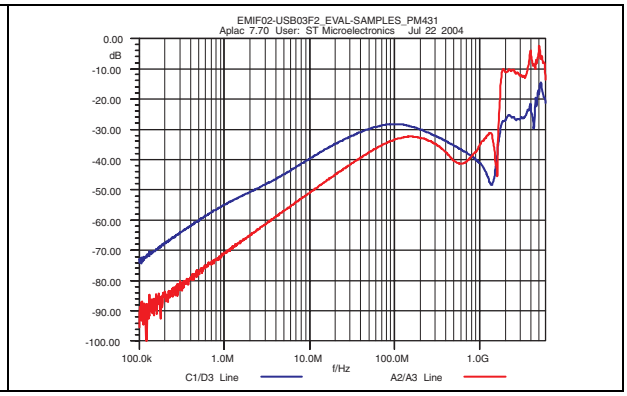


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input V(in) and on one output V(out)

Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input V(in) and on one output V(out)

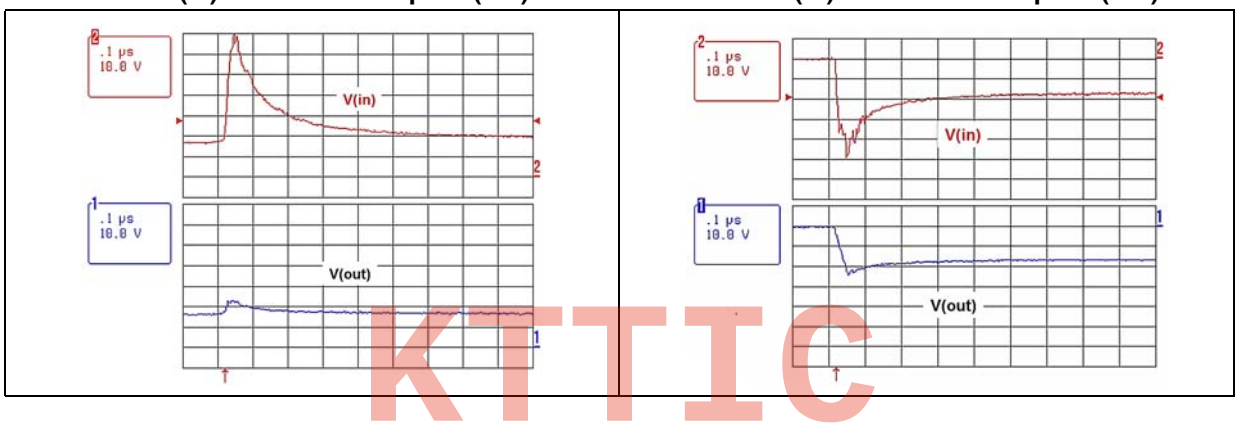
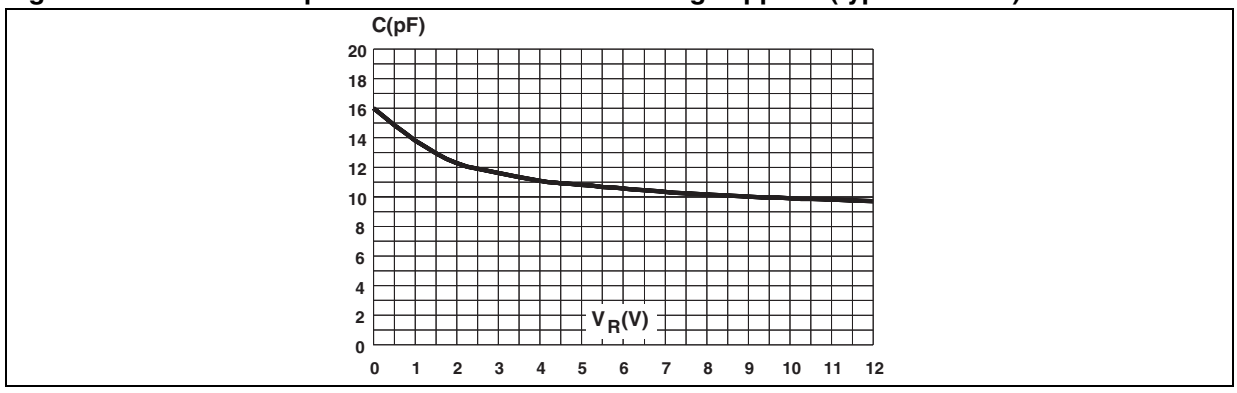


Figure 7. Junction capacitance versus reverse voltage applied (typical values)



2 Application information

Figure 8. Application schematic

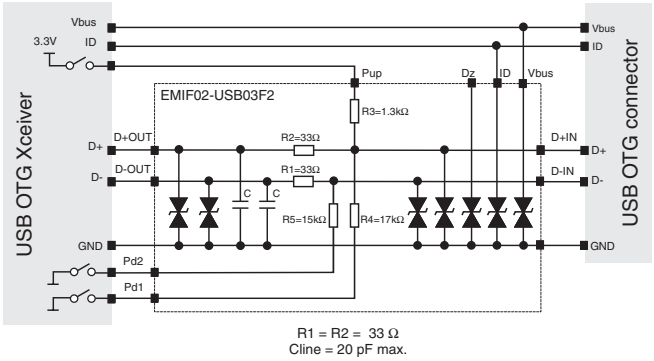


Figure 9. Aplac model

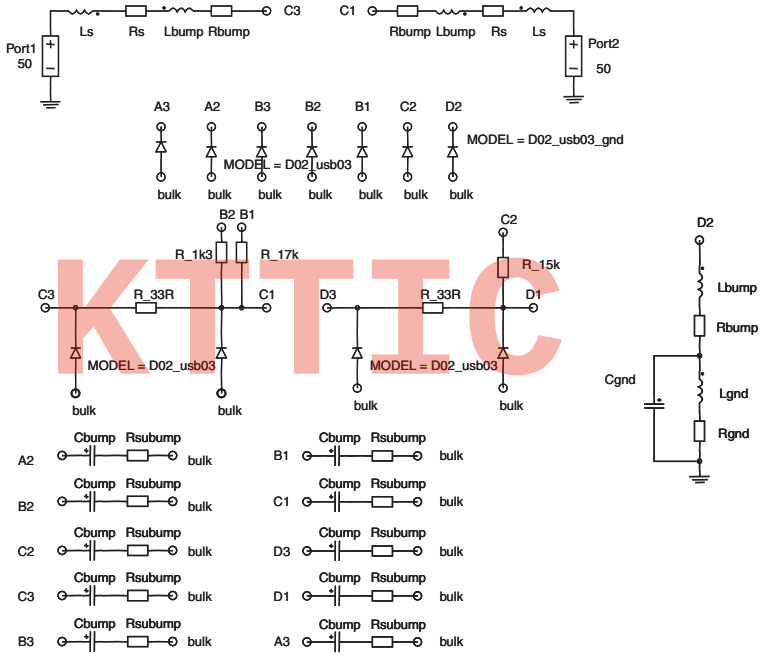
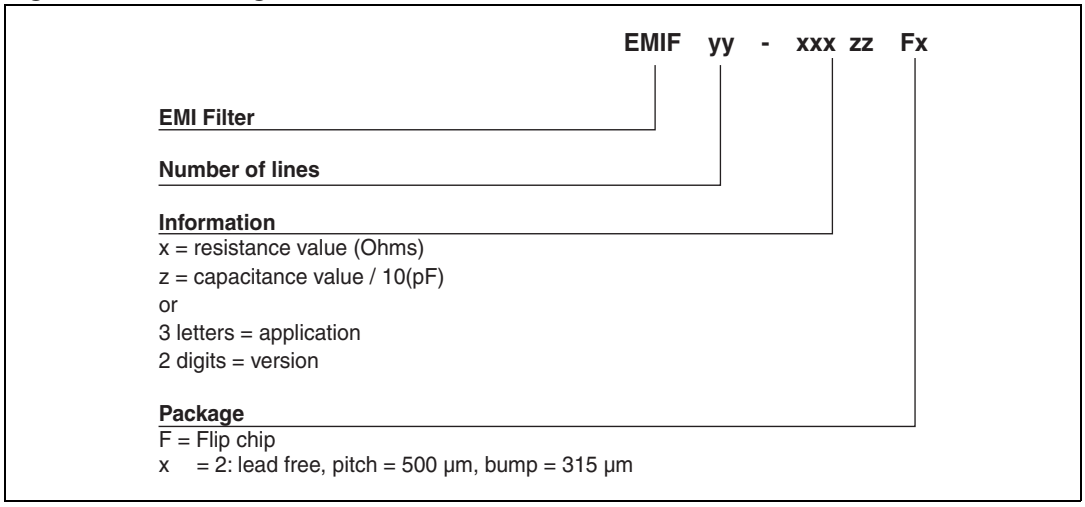


Figure 10. Aplac parameters

Ls 950pH	Rs_usb03_gnd 0.9
Rs 150m	Lgnd 50pH
R_33R 33	Rgnd 100m
R_1k3 1.3k	Cgnd 0.15pF
R_15k 15k	Lbump 50pH
R_17k 17k	Rbump 20m
Cz_usb03 11pF	Cbump 2.4pF
Rs_usb03 1	Rsubump 100m
Cz_usb03_gnd 220pF	

3 Ordering information scheme

Figure 11. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Figure 12. Package dimensions

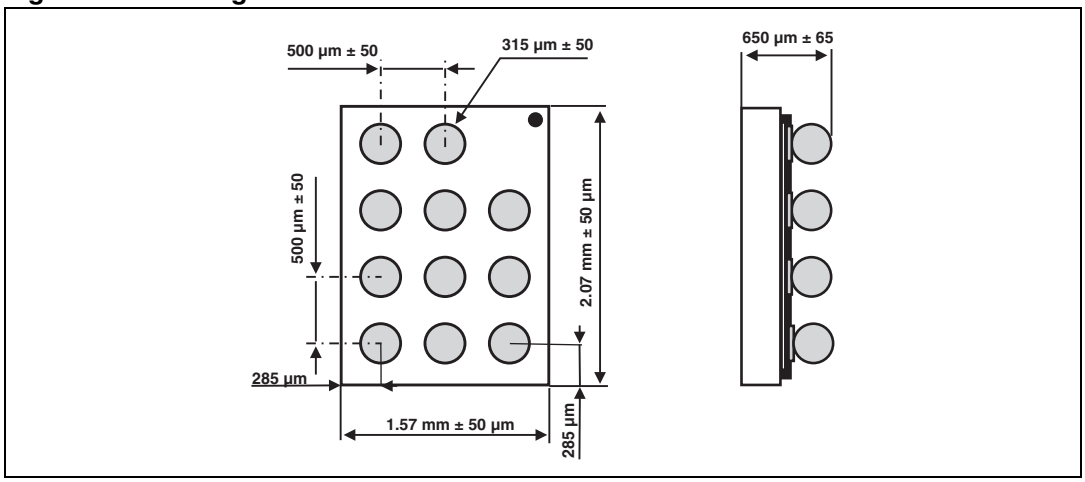


Figure 13. Footprint

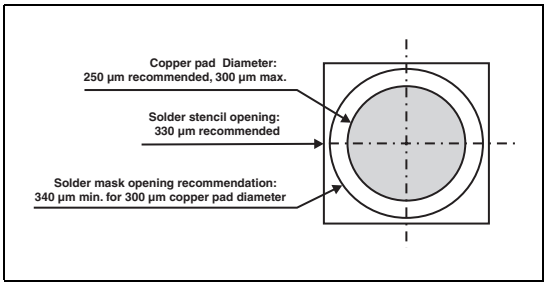


Figure 14. Marking

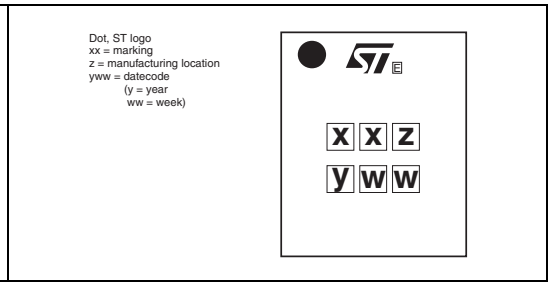
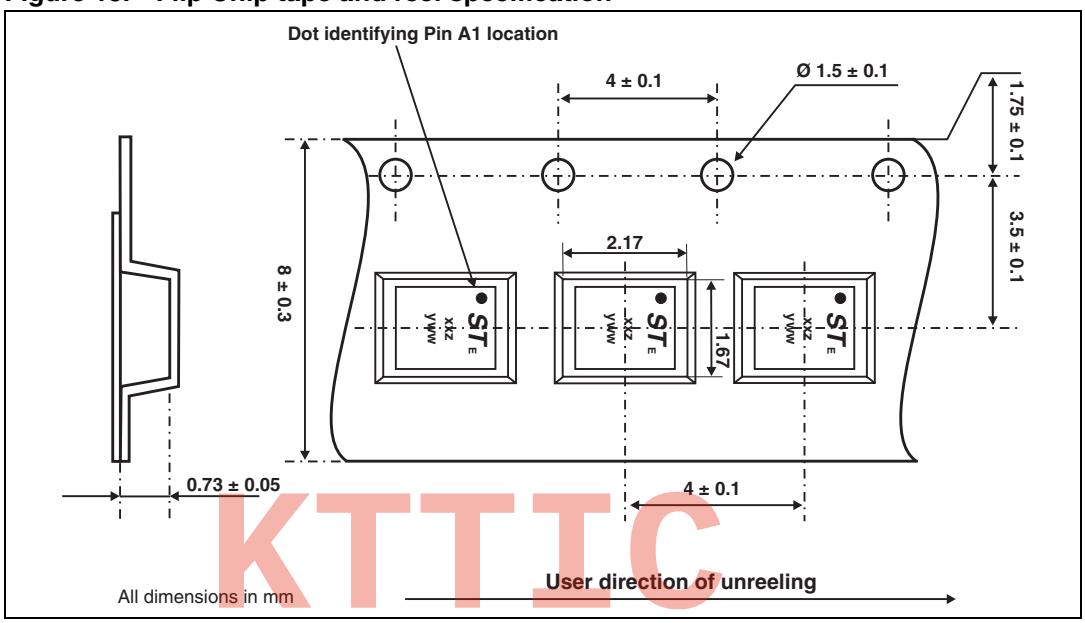


Figure 15. Flip Chip tape and reel specification



Note: More information is available in the application notes:
AN1235:"Flip Chip: Package description and recommendations for use"
AN1751: "EMI filters: Recommendations and measurements"

5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-USB03F2	FU	Flip Chip	4.5 mg	5000	Tape and reel 7"

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
14-Oct-2004	1	Initial release.
25-Oct-2004	2	*Figure 14.*: Flip Chip marking dimensions updated.
27-Oct-2004	3	Minor layout update. No content change.
28-Apr-2008	4	Updated ECOPACK statement. Updated *Figure 11*, *Figure 12*, *Figure 13*, *Figure 14* and *Figure 15.* Reformatted to current standards.

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