P87C591 Microcontroller

Program/Verify Specifications

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Philips
Semiconductors

Table 1 **PIN DESCRIPTION**:**PIN DESCRIPTION**:

PLCC 44	QFP 44	PIN NAME	NAME DURING PROG.	I/O	FUNCTION DURING PROGRAMMING
1	**39**	**AVSS**	**AVSS**		**Ground**
2	40	P1.0	A0	I	Address input 0
3	41	P1.1	A1	I	Address input 1
4	42	P1.2	A2	I	Address input 2
5	43	P1.3	A3	I	Address input 3
6	44	P1.4	A4	I	Address input 4
7	1	P1.5	A5	I	Address input 5
8	2	P1.6	A6	I	Address input 6
9	3	P1.7	A7	I	Address input 7
10	**4**	**$\overline{\text{RST}}$**	**$\overline{\text{RST}}$**	**I**	**Reset always connected LOW**
11	5	P3.0			
12	**6**	**PWM0**			
13	7	P3.1			
14	8	P3.2			
15	9	P3.3			
16	10	P3.4			
17	11	P3.5			
18	12	P3.6	P3.6	I	Mode select
19	13	P3.7	P3.7	I	Mode select
20	14	XTAL2	XTAL2	O	Clock out
21	15	XTAL1	XTAL1	I	Clock in
22	16	V_{SS}	V_{SS}	P	Ground
23	**17**	**V_{DD}**	**V_{DD}**	**P**	**+5V**
24	18	P2.0	A8	I	Address input 8
25	19	P2.1	A9	I	Address input 9
26	20	P2.2	A10	I	Address input 10
27	21	P2.3	A11	I	Address input 11
28	22	P2.4	A12	I	Address input 12
29	23	P2.5	A13	I	Address input 13
30	24	P2.6	P2.6	I	Mode select
31	25	P2.7	P2.7	I	Mode select
32	26	$\overline{\text{PSEN}}$	$\overline{\text{PSEN}}$	I	$\overline{\text{PSEN}}$ always connected to Low
33	27	ALE	$\overline{\text{PROG}}$	I	Five active Low Programming pulses
34	**28**	**PWM1**			
35	29	$\overline{\text{EA}}$	V_{PP}/V_{IH}		12.75V or 5V
36	30	P0.7	D7	I/O	Data
37	31	P0.6	D6	I/O	Data
38	32	P0.5	D5	I/O	Data
39	33	P0.4	D4	I/O	Data
40	34	P0.3	D3	I/O	Data
41	35	P0.2	D2	I/O	Data
42	36	P0.1	D1	I/O	Data
43	37	P0.0	D0	I/O	Data
44	**38**	**AV_{REF+}**	**AV_{REF+}**	**P**	**+5V**

Table 2 :**Product ID**

PRODUCT	EPROM SIZE	END ADDRESS	SIGNATURE BYTES 30H	31H	60H	SECURITY BITS 1	2	3
P87C591	16K x 8	3FFFH	15H	98H	01H	Y	Y	Y

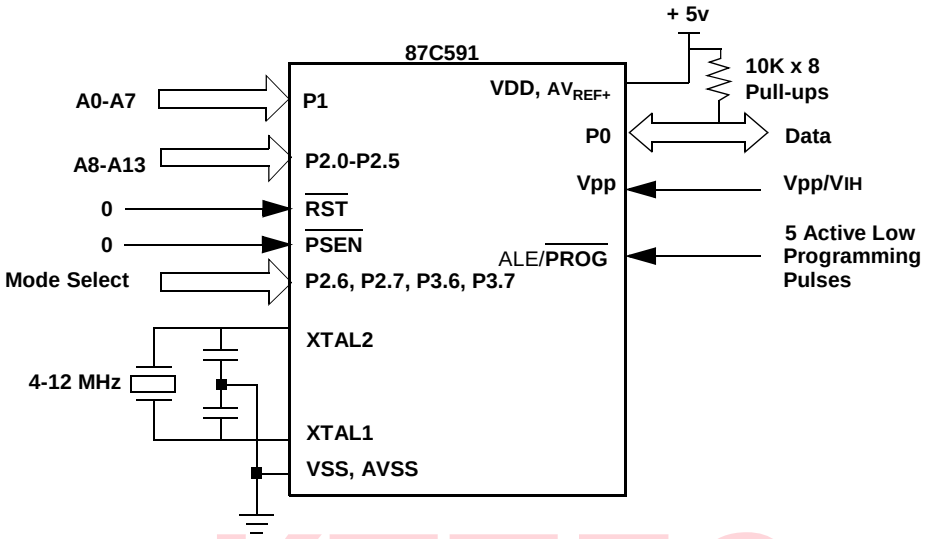


Figure 1. Programming/Verify connection

Note:

1. All address pins have to be driven, some P1 pins do not have pullups and should not be left open.

Clock in

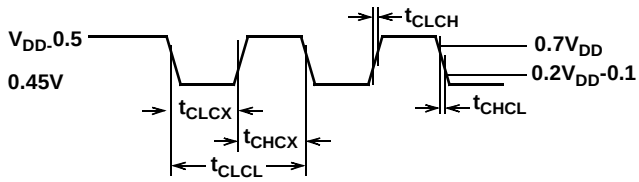


Figure 2. Clock Timing Waveform

Table 3 :**Programming modes**

MODE	$\overline{R}$ $\overline{S}$ $\overline{T}$	$\overline{P}$ $\overline{S}$ $\overline{E}$ $\overline{N}$	ALE/$\overline{PROG}$	VPP	MODE SELECT P2.7	P2.6	P3.7	P3.6	ADDRESS A[13:0] INPUT	DATA D[7:0] I/O
Read Signature Byte 1	0	0	1	1	$\overline{EV}$	0	0	0	30H	Sig.1 out
Read Signature Byte 2	0	0	1	1	$\overline{EV}$	0	0	0	31H	Sig.2 out
Read Signature Byte 3	0	0	1	1	$\overline{EV}$	0	0	0	60H	Sig.3 out
Program code	0	0	NP	V_{PP}	1	0	1	1	Byte Address	Byte Data In
Verify code	0	0	1	1	$\overline{EV}$	0	1	1	Byte Address	Byte Data Out
Program Encryption byte	0	0	NP	V_{PP}	1	0	1	0	0 to 3FH	Byte Data In
Program Security bit 1	0	0	NP	V_{PP}	1	1	1	1	X	X
Program Security bit 2	0	0	NP	V_{PP}	1	1	0	0	X	X
Program Security bit 3	0	0	NP	V_{PP}	$\overline{EV}$	1	0	1	X	X
Verify Security bits	0	0	1	1	$\overline{EV}$	0	1	0	X	Data Out

Notes:

1. "0" = Valid V_{IL} "1" = Valid V_{IH}
2. V_{PP} = 12.75V ±0.25V
3. V_{DD} = 5V ±0.5V
4. NP = 5 Negative Pulses
5. $\overline{EV}$ = Enable Verify

Reading Signature bytes

The 3 signature bytes are assigned by Philips to uniquely identify each product. The signature bytes are read out of locations 030H, 031H and 060H. The signature bytes can only be verified, they cannot be programmed by the programmer.

1. Connect V_{DD} = 5V, V_{PP} = 5V, Connect a a crystal to pins XTAL1 and XTAL2 or a clock to XTAL1 pin.
2. Connect the mode select inputs as specified in Table 3 for reading signature bytes.
3. Apply Address = 30H; toggle P2.7 from 1 to 0, to enable verify; wait 24 clock cycles (minimum) and read the signature byte on port 0.
4. Repeat reading from address 31H and 60H.

Verify EPROM

1. Connect V_{DD} = 5V, V_{PP} = 5V, Connect a a crystal to pins XTAL1 and XTAL2 or a clock to XTAL1 pin.
2. Connect the mode select inputs as specified at Table 3 for code verify.
3. Apply Address = 0H; toggle P2.7 from 1 to 0, to enable verify; wait 24 clock cycles (minimum) and read the code byte on port 0.

4. Repeat reading through all the Program addresses.

EPROM Programming

1. Connect V_{DD} = 5V, V_{PP} = 5V, Connect a a crystal to pins XTAL1 and XTAL2 or a clock to XTAL1 pin.
2. Connect the mode select inputs as specified at Table 3 for programming code and $\overline{PROG}$=1.
3. Wait 10µSec and change V_{PP} = 5V to V_{PP} = 12.75V
4. Apply Address and data of the programmed byte, wait 24 clock cycles (minimum).
5. Generate five active low pulses on pin $\overline{PROG}$ to program the byte.
6. Apply Address and data of the next programmed byte, wait 24 clock cycles (minimum).
7. Generate five active low pulses on pin $\overline{PROG}$ to program the byte.
8. repeat 6,7 for all the programmed bytes.
9. Wait 10µSec and change V_{PP} = 12.75V to V_{PP} = 5V

Encryption Table Programming

The 87C591 has a 64 byte encryption table.

1. Connect V_{DD} = 5V, V_{PP} = 5V, Connect a crystal to pins XTAL1 and XTAL2 or a clock to XTAL1 pin.
2. Connect the mode select inputs as specified at Table 3 for Encryption Table programming and $\overline{PROG}$=1.
3. Wait 10µSec and change V_{PP} = 5V to V_{PP} = 12.75V
4. Apply Address and data of the programmed byte, wait 24 clock cycles (minimum).
5. Generate five active low pulses on pin $\overline{PROG}$ to program the byte.
6. Apply Address and data of the next programmed byte, wait 24 clock cycles (minimum).
7. Generate five active low pulses on pin $\overline{PROG}$ to program the byte.
8. repeat 6,7 for all the Encryption Table bytes.
9. Wait 10µSec and change V_{PP} from 12.75V to 5V

Security bits Programming

1. Connect V_{DD} = 5V, V_{PP} = 5V, Connect a a crystal to pins XTAL1 and XTAL2 or a clock to XTAL1 pin.
2. Connect the mode select inputs as specified at Table 3 for Security bits programming and $\overline{PROG}$=1.
3. Wait 10µSec and change V_{PP} = 5V to V_{PP} = 12.75V
4. Wait 24 clock cycles (minimum).
5. Wait 10µSec and change V_{PP} from 12.75V = 5V
6. Repeat 2-5 for all the security bits.

Verify Security bits

1. Connect V_{DD} = 5V, V_{PP} = 5V, Connect a a crystal to pins XTAL1 and XTAL2 or a clock to XTAL1 pin.
2. Connect the mode select inputs as specified at Table 3 for security bits verify.
3. Toggle P2.7 from 1 to 0, to enable verify; wait 24 clock cycles (minimum) and read the byte on port 0.

Table 4 :**Security Bits**

PORT 0	SECURITY BITS
P0.7 = 0	Security bit 1 programmed
P0.7 = 1	Security bit 1 not programmed
P0.6 = 0	Security bit 2 programmed
P0.6 = 1	Security bit 2 not programmed
P0.3 = 0	Security bit 3 programmed
P0.3 = 1	Security bit 3 not programmed
P0.5 = 0	This bit is always = 0

Table 5DC Characteristics

DC CHARACTERISTIC TA = 0^{o}C to 70 ^{o}C, V_{DD} = 5V $\pm$ 5%, V_{PP} = 12.75V $\pm$ 0.25V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
IDD	VDD current		20	45	mA	
IPP	VPP current			50	mA	
VIL	Input Low Voltage	-0.5		.2*V_{DD}-0.1	V	Except P1.0, P1.1, P1.6, P1.7
VIL1	Input Low Voltage	-0.5		.2*V_{DD}-0.3	V	for $\overline{EA}$
VIL2	Input Low Voltage	-0.5		1.4	V	P1.0 and P1.1
VIL3	Input Low Voltage	-0.5		.3*V_{DD}	V	P1.6 and P1.7
VIH	Input High Voltage	.2VDD +.9		VDD+0.5V	V	Except P1.0, P1.1, P1.6, P1.7, XTAL1, $\overline{RST}$
VIH1	Input High Voltage	.7VDD		VDD+0.5V	V	XTAL1, $\overline{RST}$
VIH2	Input High Voltage	3		VDD+0.5V	V	P1.0, P1.1
VIH3	Input High Voltage	.7VDD		6V	V	P1.6, P1.7

NOTES:

1. V_{DD} must be applied before V_{PP} and removed after V_{PP}.
2. VPP must not exceed 13V including overshoot.
3. V_{IH} is for pins P0, P1, P2, P3, $\overline{EA}$
4. $V_{IH}1$ is for pins XTAL1, $\overline{RST}$

Table 6 - AC Characteristics for P87C591

AC CHARACTERISTIC TA = 0°C to 70 °C, VDD = 5V ± 5%, VPP = 12.75V ± 0.25V

SYMBOL	PARAMETER	MIN	MAX	UNIT
1/tCLCL	Oscillator/Clock frequency	3.5	12	MHz
tCHCX	XTAL1 CLK High	20		nSec
tCLCX	XTAL1 CLK Low	20		nSec
tCLCH	XTAL1 CLK rise time		20	nSec
tCHCL	XTAL1 CLK fall time		20	nSec
tAVGL	Address setup to PROG Low	24*tCLCL		
tGHAX	Address hold after PROG change	24*tCLCL		
tDVGL	Data setup to PROG Low	24*tCLCL		
tGHDX	Data hold after PROG change	24*tCLCL		
tEHSH	P2.7 (ENABLE) High to VPP High	24*tCLCL		
tSHGL	VPP setup to PROG Low	10		µSec
tGHSL	VPP hold after PROG	10		µSec
tGLGH	PROG pulse width	40	60	µSec
tAVQV	Address to Valid data	7*tCLCL	24*tCLCL	
tELQV	P2.7 (ENABLE) Low to valid data	18*tCLCL	24*tCLCL	
tEHQZ	Data float after P2.7 (ENABLE) High	18*tCLCL	24*tCLCL	
tGHGL	PROG High to PROG Low	10		µSec

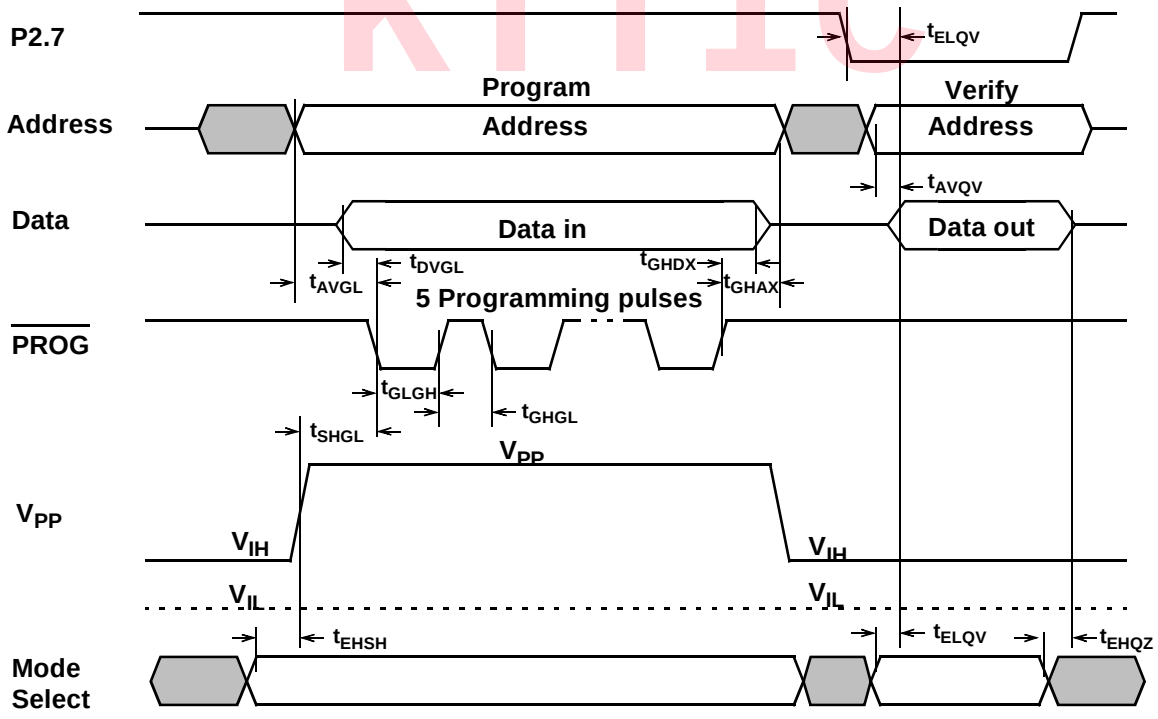


Figure 3. Program/Verify Timings

6 PINNING INFORMATION

6.1 Pinning diagram

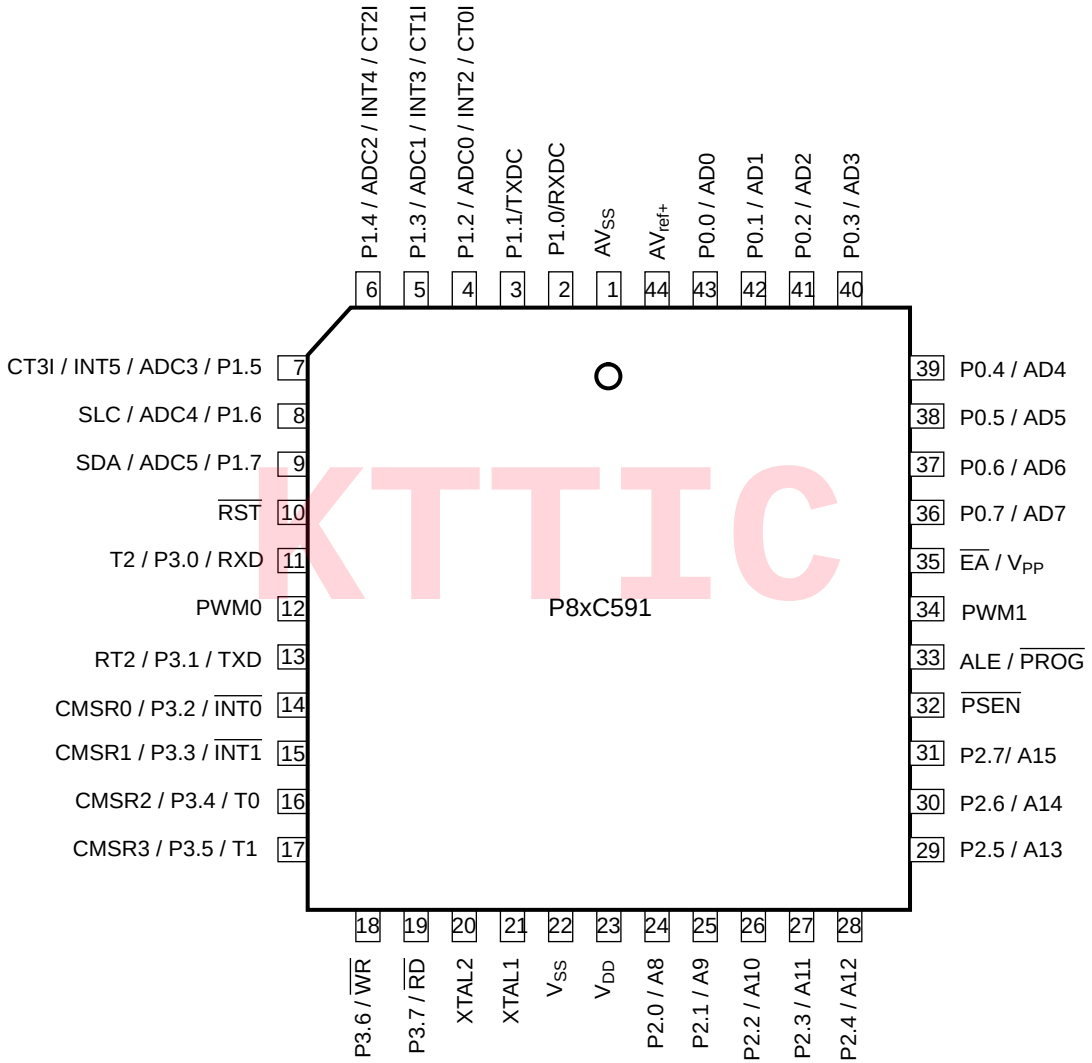
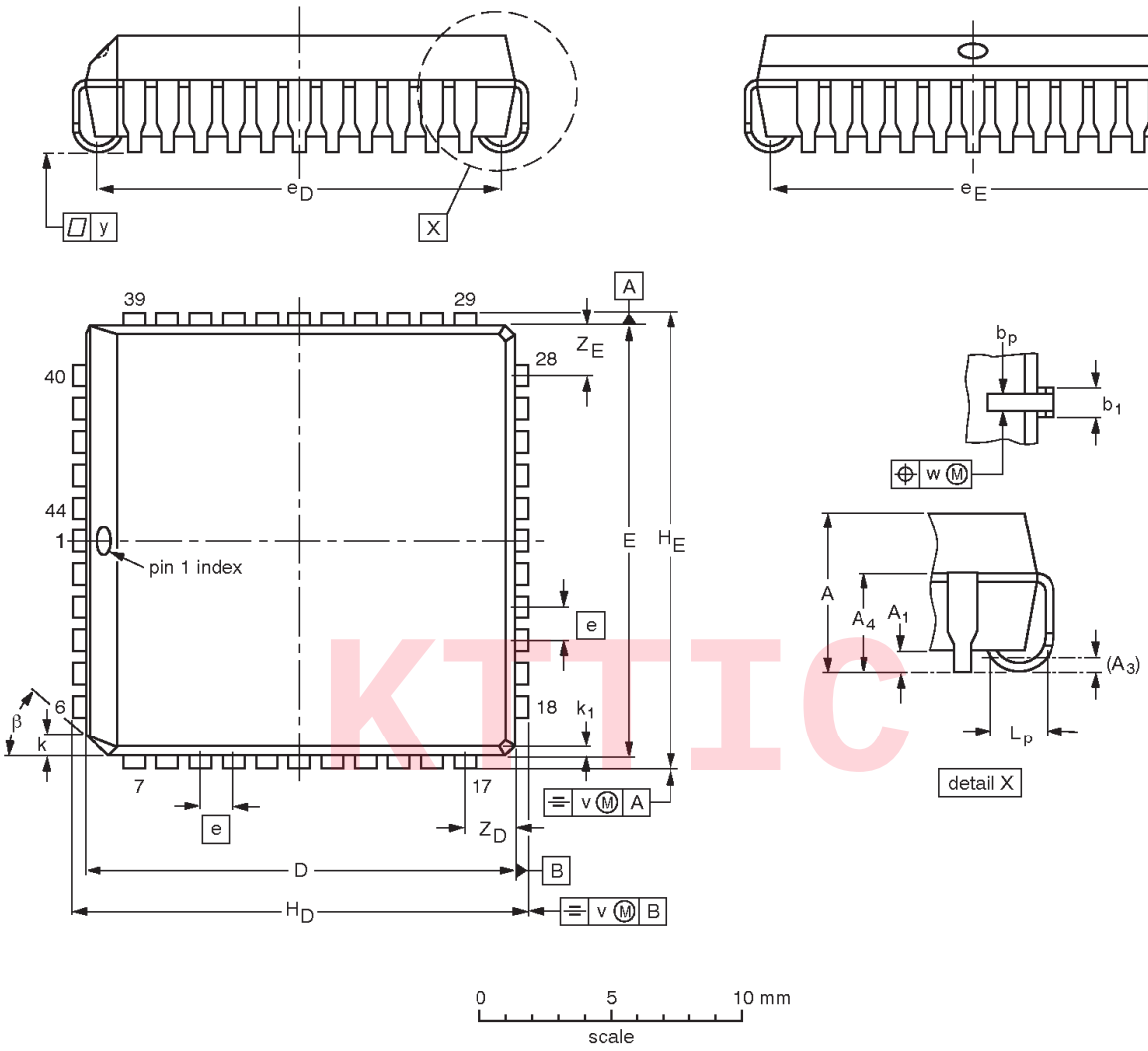


Fig.3 Pinning Diagram for 44-lead LCC Package.

Package outlines

PLCC44: plastic leaded chip carrier; 44 leads SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~95-02-25~~ 97-12-16

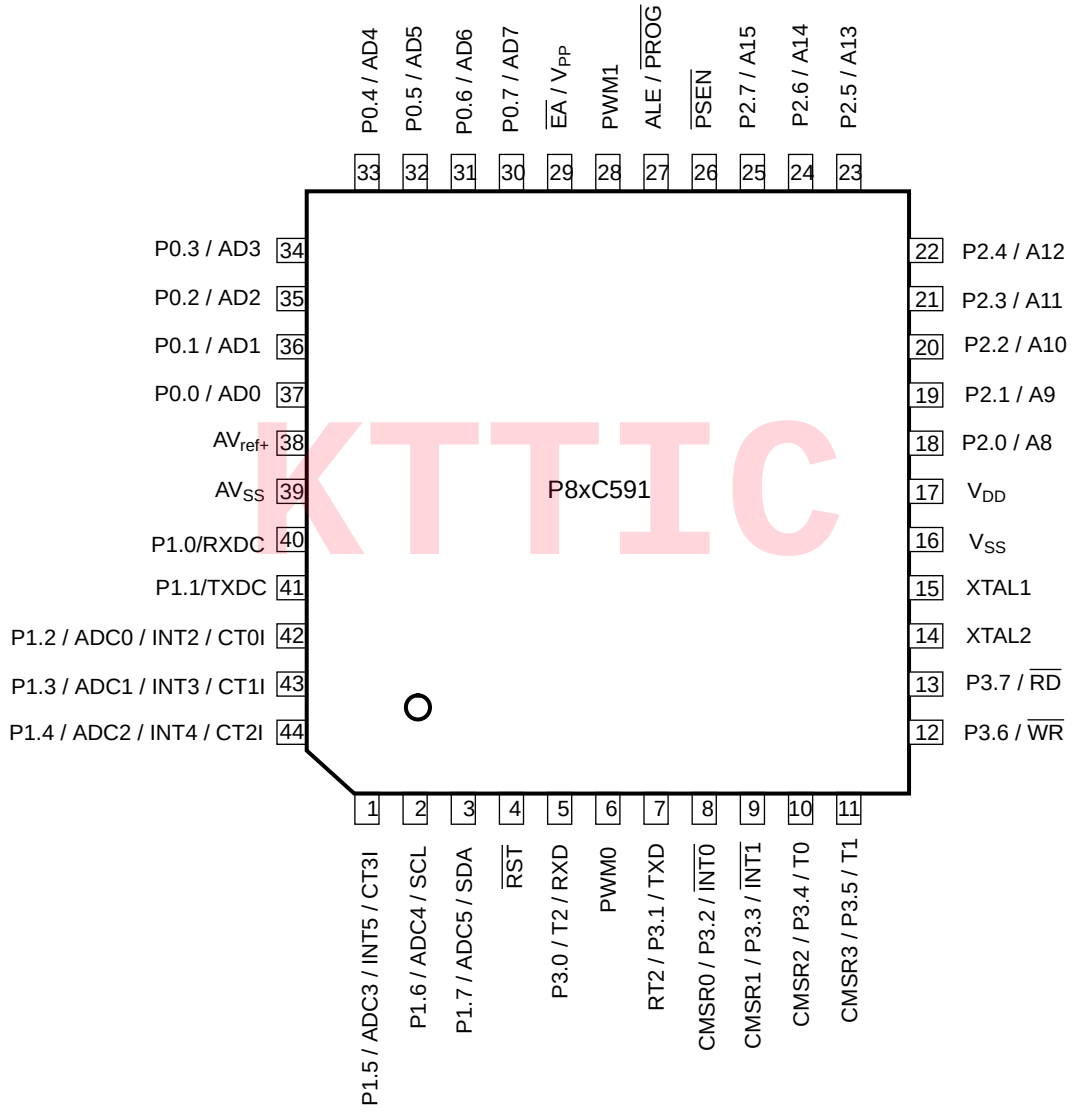
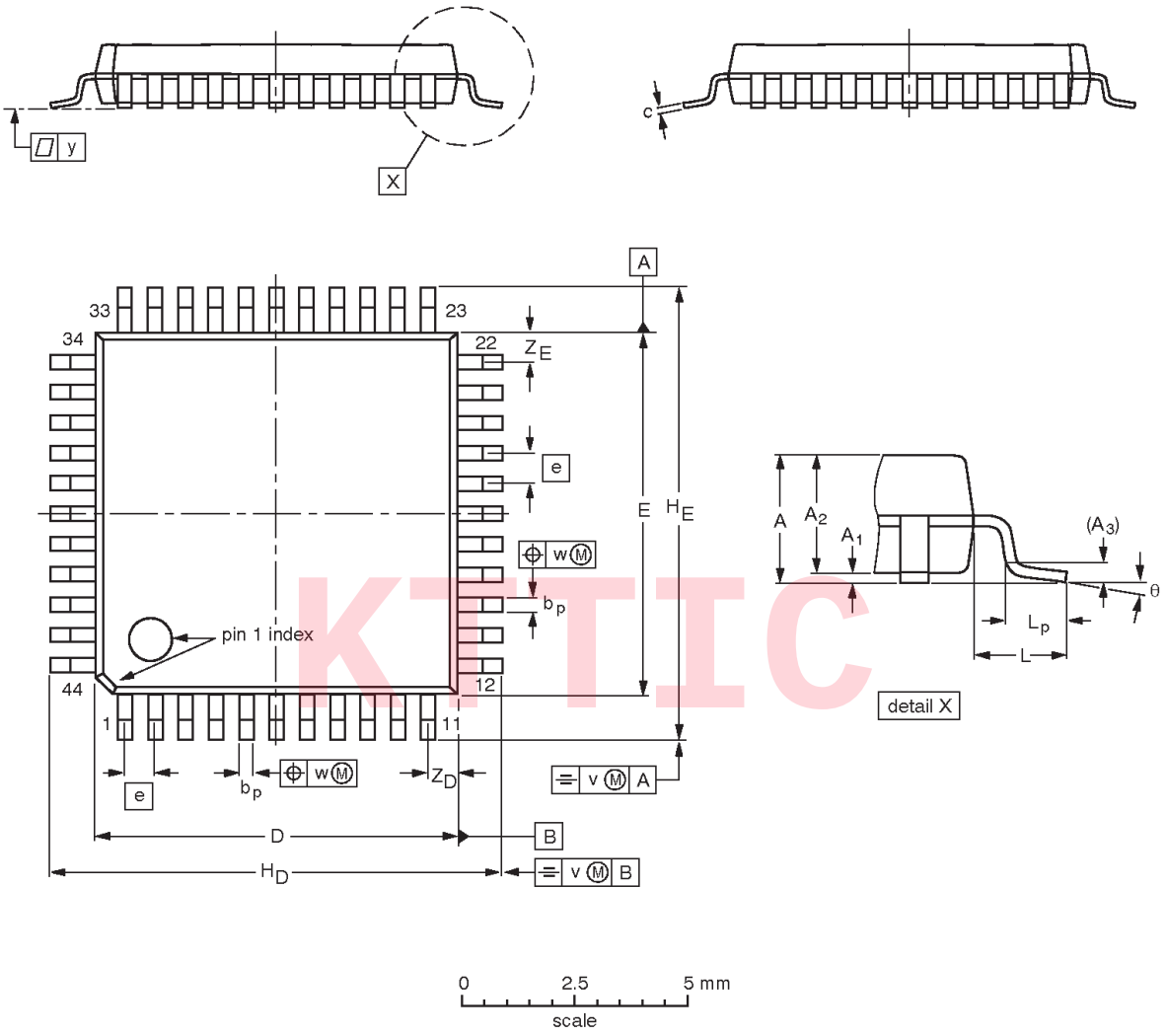


Fig.4 Pinning Diagram for 44-lead Plastic Quad Flat Package (QFP).

Package outlines

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01