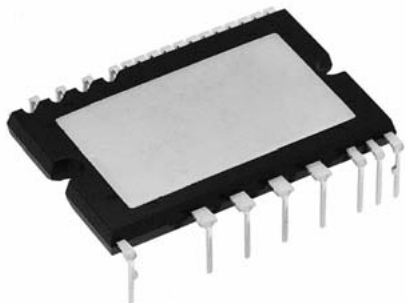


PS21963-ET/-AET/-CET/-ETW

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21963-ET



INTEGRATED POWER FUNCTIONS

600V/8A low-loss CSTBT™ inverter bridge for three phase DC-to-AC power conversion

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

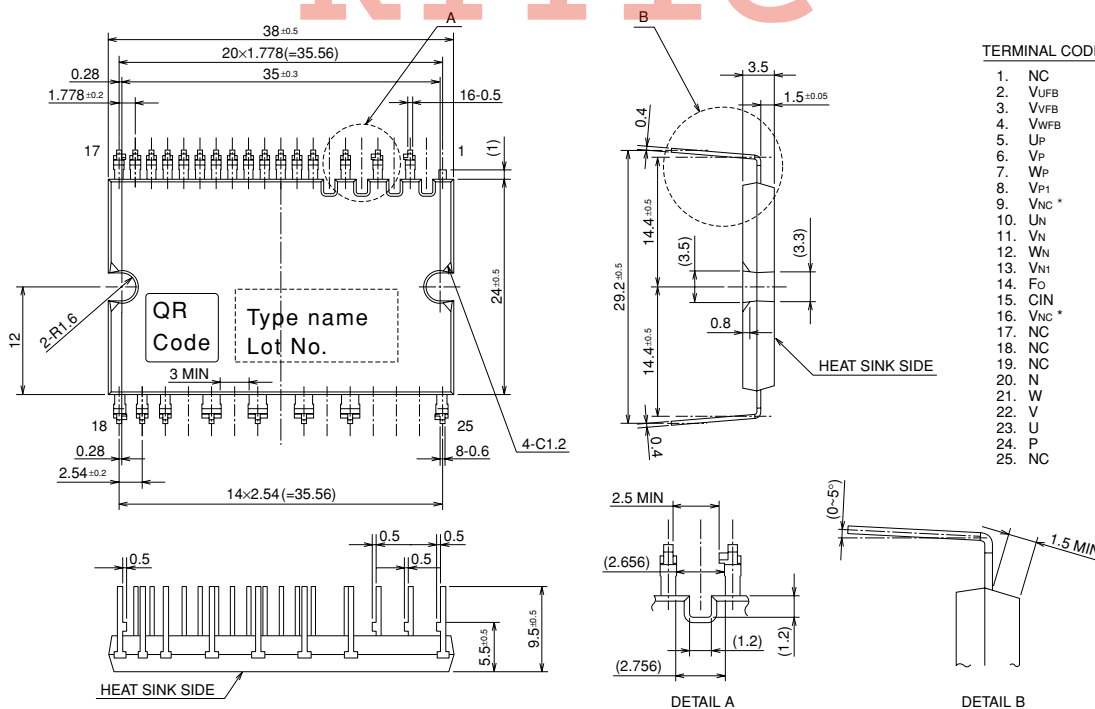
- For upper-leg IGBTs : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC), Over temperature protection (OT).
- Fault signaling : Corresponding to an SC fault (Lower-leg IGBT), a UV fault (Lower-side supply) or an OT fault (LVIC temperature).
- Input interface : 3V, 5V line (High Active).
- UL Approved : Yellow Card No. E80276

APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES (PS21963-ET)

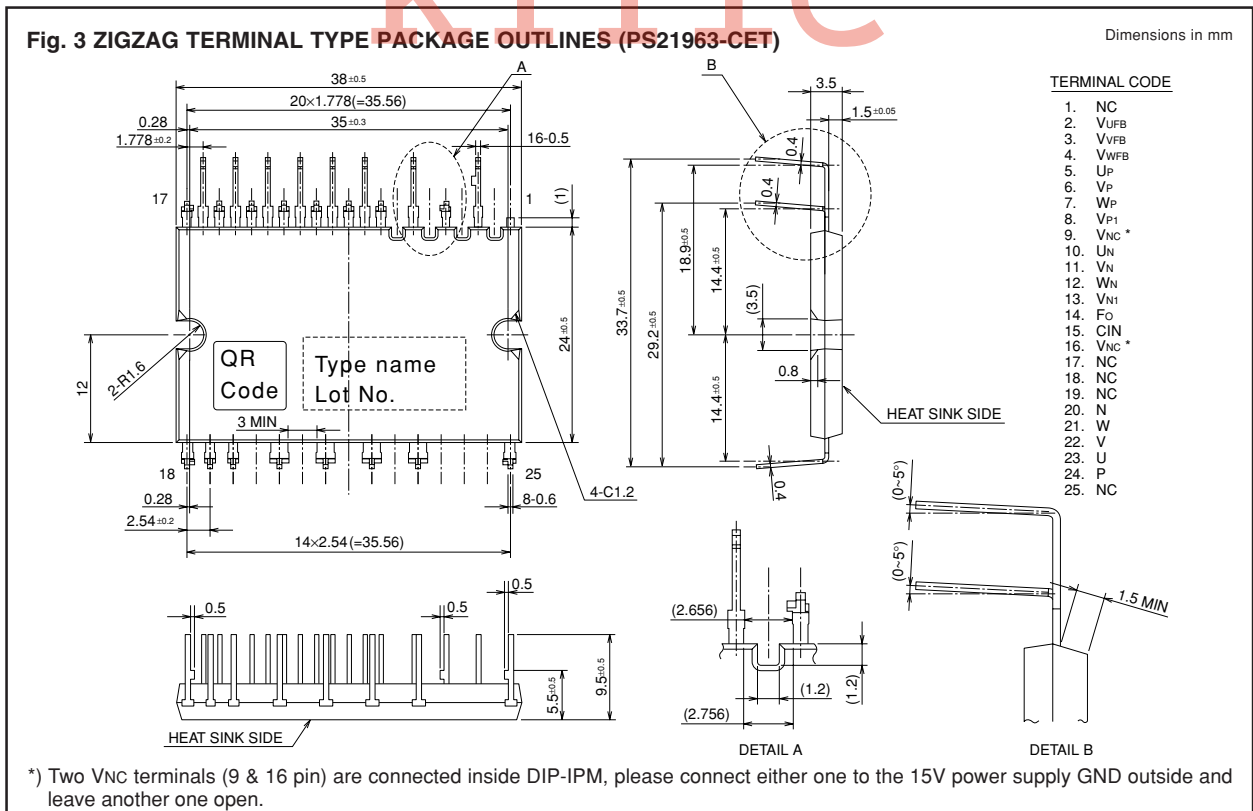
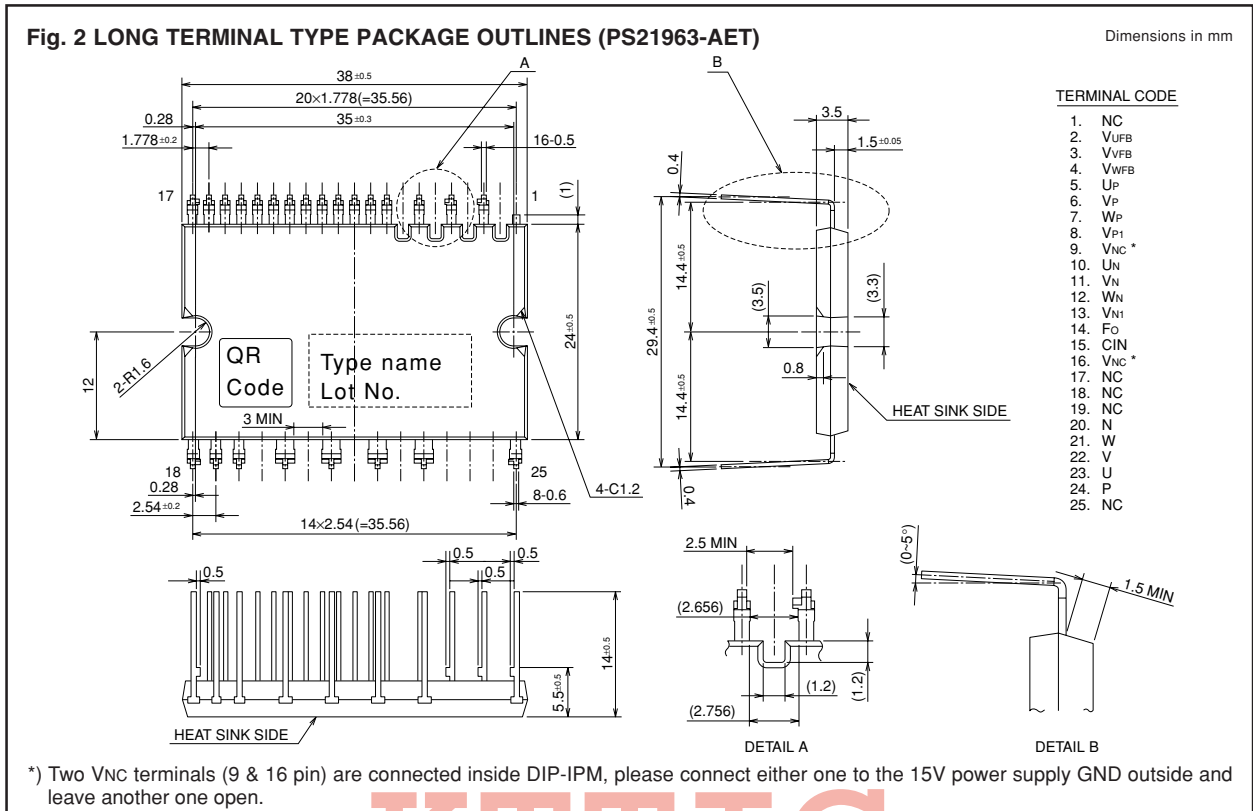
Dimensions in mm



*) Two V_{NC} terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.

PS21963-ET/-AET/-CET/-ETW

**TRANSFER-MOLD TYPE
INSULATED TYPE**

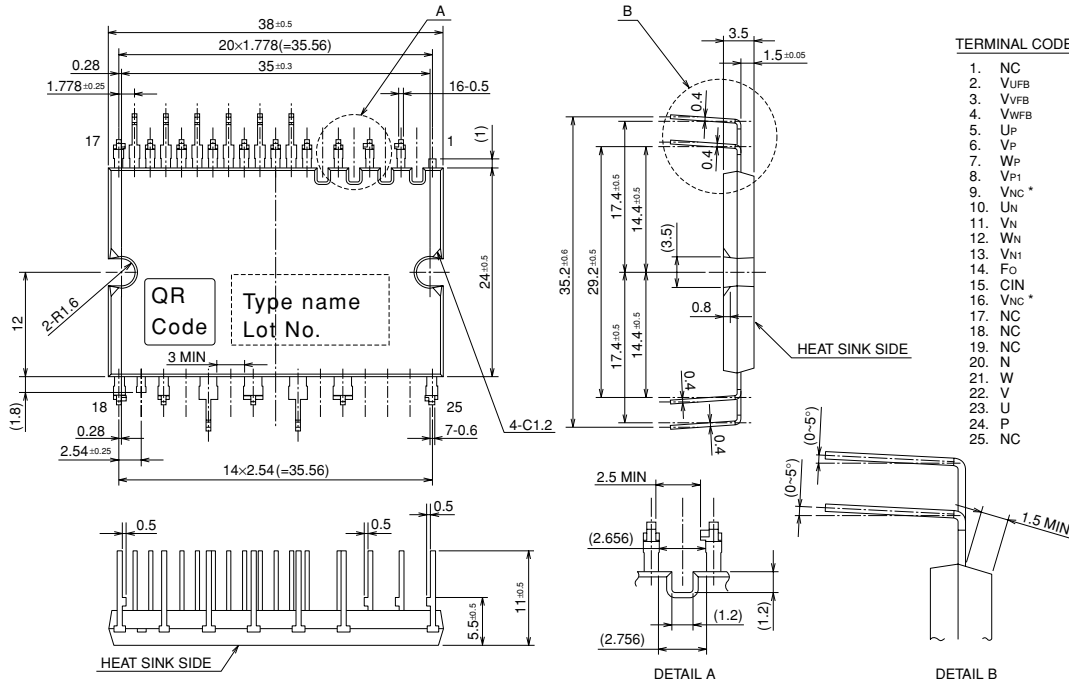


PS21963-ET/-AET/-CET/-ETW

TRANSFER-MOLD TYPE
INSULATED TYPE

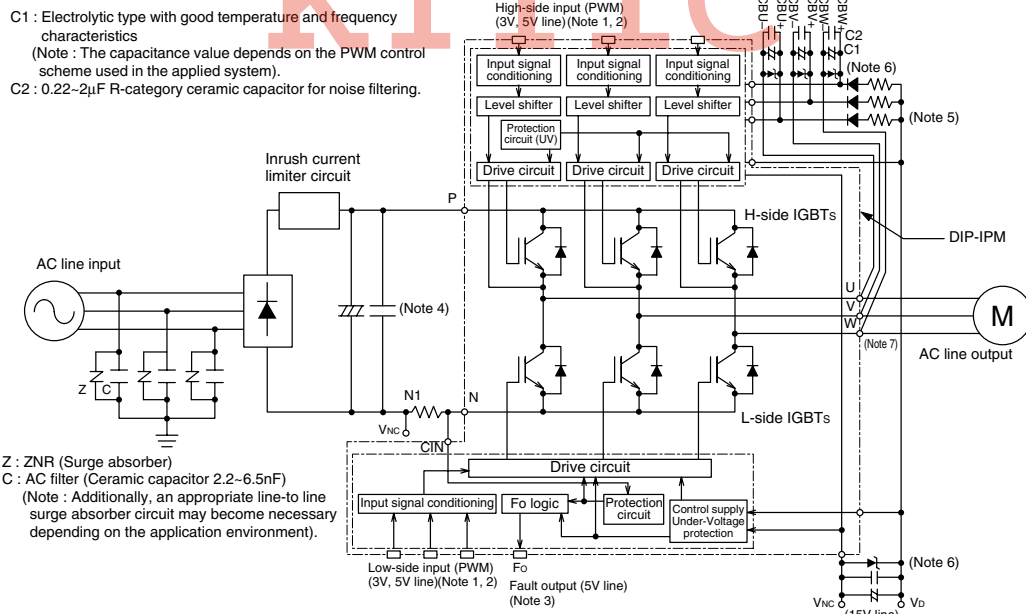
Fig. 4 BOTH SIDES ZIGZAG TERMINAL TYPE PACKAGE OUTLINES (PS21963-ETW)

Dimensions in mm



*) Two V_{NC} terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.

Fig. 5 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

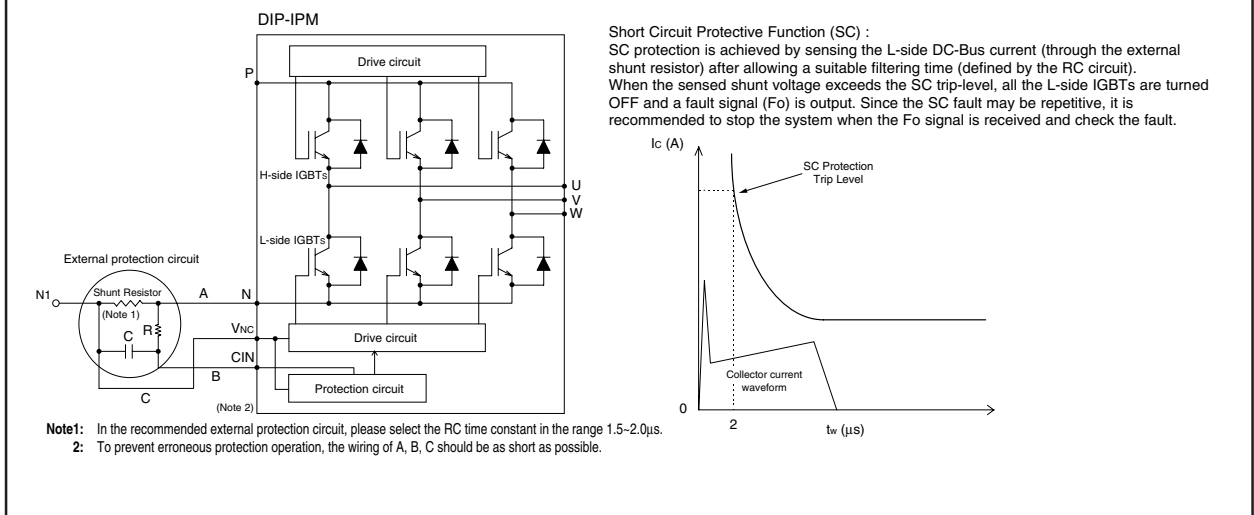


- Note1:** Input logic is high-active. There is a 3.3kΩ (min) pull-down resistor built-in each input circuit. When using an external CR filter, please make it satisfy the input threshold voltage.
- 2:** By virtue of integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible. (see also Fig. 11)
- 3:** This output is open drain type. The signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor. (see also Fig. 11)
- 4:** The wiring between the power DC link capacitor and the P, N1 terminals should be as short as possible to protect the DIP-IPM against catastrophic high surge voltages. For extra precaution, a small film type snubber capacitor (0.1-0.22μF, high voltage type) is recommended to be mounted close to these P & N1 DC power input pins.
- 5:** High voltage (600V or more) and fast recovery type (less than 100ns) diodes should be used in the bootstrap circuit.
- 6:** It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
- 7:** Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.

PS21963-ET/-AET/-CET/-ETW

**TRANSFER-MOLD TYPE
INSULATED TYPE**

Fig. 6 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
VCC	Supply voltage	Applied between P-N	450	V
VCC(surge)	Supply voltage (surge)	Applied between P-N	500	V
VCEs	Collector-emitter voltage		600	V
$\pm I_c$	Each IGBT collector current	$T_c = 25^\circ\text{C}$	8	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_c = 25^\circ\text{C}$, less than 1ms	16	A
Pc	Collector dissipation	$T_c = 25^\circ\text{C}$, per 1 chip	24.3	W
Tj	Junction temperature	(Note 1)	-20~+125	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C ($@ T_c \leq 100^\circ\text{C}$). However, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \leq 125^\circ\text{C}$ ($@ T_c \leq 100^\circ\text{C}$).

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
Vd	Control supply voltage	Applied between VP1-VNC, VN1-VNC	20	V
VDB	Control supply voltage	Applied between VUFB-U, VVFB-V, VWFB-W	20	V
VIN	Input voltage	Applied between UP, VP, WP, UN, VN, WN-VNC	-0.5~Vd+0.5	V
VFO	Fault output supply voltage	Applied between Fo-VNC	-0.5~Vd+0.5	V
Ifo	Fault output current	Sink current at Fo terminal	1	mA
Vsc	Current sensing input voltage	Applied between CIN-VNC	-0.5~Vd+0.5	V

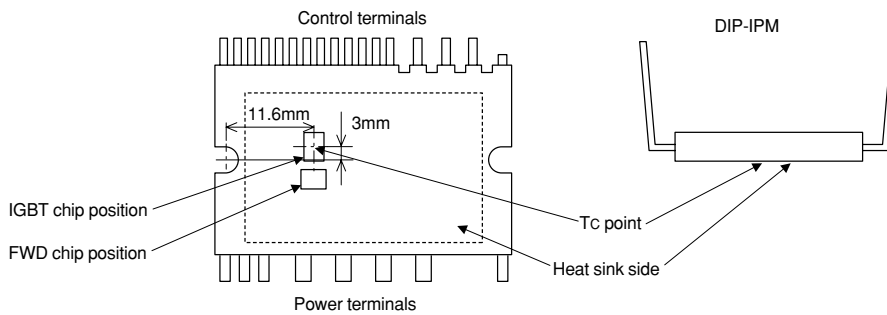
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**TRANSFER-MOLD TYPE
INSULATED TYPE**

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(PROT)}	Self protection supply voltage limit (short circuit protection capability)	V _D = 13.5~16.5V, Inverter part T _j = 125°C, non-repetitive, less than 2μs	400	V
T _C	Module case operation temperature	(Note 2)	-20~+100	°C
T _{stg}	Storage temperature		-40~+125	°C
V _{iso}	Isolation voltage	60Hz, Sinusoidal, 1 minute, Between pins and heat-sink plate	1500	V _{rms}

Note 2: T_C measurement point



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case thermal resistance	Inverter IGBT part (per 1/6 module)	—	—	4.1	°C/W
R _{th(j-c)F}	Junction to case thermal resistance (Note 3)	Inverter FWD part (per 1/6 module)	—	—	5.4	°C/W

Note 3: Grease with good thermal conductivity should be applied evenly with about +100μm~+200μm on the contacting surface of DIP-IPM and heat-sink.

The contacting thermal resistance between DIP-IPM case and heat sink (R_{th(c-f)}) is determined by the thickness and the thermal conductivity of the applied grease. For reference, R_{th(c-f)} (per 1/6 module) is about 0.3°C/W when the grease thickness is 20μm and the thermal conductivity is 1.0W/m·k.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CE(sat)}	Collector-emitter saturation voltage	V _D = V _{DB} = 15V V _{IN} = 5V	—	1.70	2.20	V
V _{EC}	FWD forward voltage	T _j = 25°C, -I _C = 8A, V _{IN} = 0V	—	1.80	2.30	
t _{on}	Switching times	V _{CC} = 300V, V _D = V _{DB} = 15V I _C = 8A, T _j = 125°C, V _{IN} = 0 ↔ 5V Inductive load (upper-lower arm)	0.60	1.10	1.70	μs
t _{tr}			—	0.30	—	μs
t _{c(on)}			—	0.40	0.60	μs
t _{off}			—	1.40	2.00	μs
t _{c(off)}			—	0.40	0.75	μs
I _{CES}	Collector-emitter cut-off current	V _{CE} = V _{CES}	—	—	1	mA
		T _j = 125°C	—	—	10	

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**TRANSFER-MOLD TYPE
INSULATED TYPE**

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I _D	Circuit current	V _D = V _{DB} = 15V V _{IN} = 5V	Total of V _{P1} -V _{NC} , V _{N1} -V _{NC}	—	—	2.80	mA
			V _{UFB-U} , V _{VFB-V} , V _{WFB-W}	—	—	0.55	mA
		V _D = V _{DB} = 15V V _{IN} = 0V	Total of V _{P1} -V _{NC} , V _{N1} -V _{NC}	—	—	2.80	mA
			V _{UFB-U} , V _{VFB-V} , V _{WFB-W}	—	—	0.55	mA
V _{FOH}	Fault output voltage	V _{SC} = 0V, F _O terminal pull-up to 5V by 10kΩ	4.9	—	—	V	
V _{FOL}		V _{SC} = 1V, I _{FO} = 1mA	—	—	0.95	V	
V _{SC(ref)}	Short circuit trip level	T _j = 25°C, V _D = 15V (Note 4)	0.43	0.48	0.53	V	
I _{IN}	Input current	V _{IN} = 5V	0.70	1.00	1.50	mA	
OT _t	Over temperature protection (Note 5)	V _D = 15V, At temperature of LVIC	Trip level	100	120	140	°C
OT _{rh}			Trip/reset hysteresis	—	10	—	
UV _{DBt}	Control supply under-voltage protection	T _j ≤ 125°C	Trip level	10.0	—	12.0	V
UV _{DBr}			Reset level	10.5	—	12.5	V
UV _{Dt}			Trip level	10.3	—	12.5	V
UV _{Dr}			Reset level	10.8	—	13.0	V
t _{FO}	Fault output pulse width	(Note 6)	20	—	—	μs	
V _{th(on)}	ON threshold voltage	Applied between UP, VP, WP, UN, VN, WN-VNC	—	2.1	2.6	V	
V _{th(off)}	OFF threshold voltage		0.8	1.3	—	V	
V _{th(hys)}	ON/OFF threshold hysteresis voltage		0.35	0.65	—	V	

Note 4: Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

5: Over temperature protection (OT) outputs fault signal, when the LVIC temperature exceeds OT trip temperature level (OT_t). In that case if the heat sink comes off DIP-IPM or fixed loosely, don't reuse that DIP-IPM. (There is a possibility that junction temperature of power chips exceeded maximum T_j (150°C)).

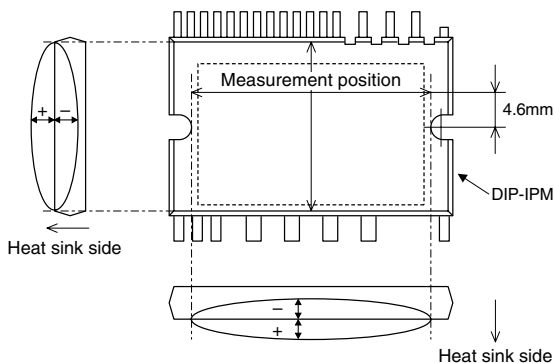
6: Fault signal is asserted only corresponding to a SC, a UV or an OT failure at lower side, and the F_O pulse width is different for each failure modes. For SC failure, F_O output is with a fixed width of 20μsec(min), but for UV or OT failure, F_O output continuously during the whole UV or OT period, however, the minimum F_O pulse width is 20μsec(min) for very short UV or OT period less than 20μsec.

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Limits			Unit
		Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 7) Recommended : 0.69 N·m	0.59	—	0.78	N·m
Weight		—	10	—	g
Heat-sink flatness	(Note 8)	-50	—	100	μm

Note 7: Plain washers (ISO 7089~7094) are recommended.

Note 8: Flatness measurement position



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**TRANSFER-MOLD TYPE
INSULATED TYPE**

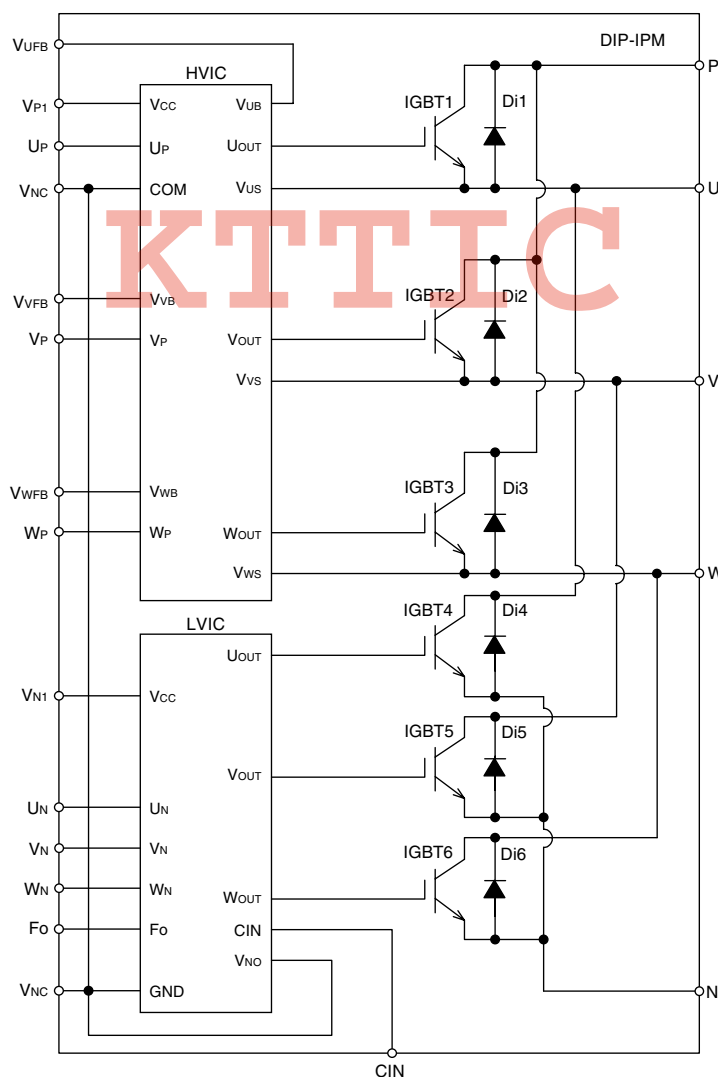
RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
VCC	Supply voltage	Applied between P-N	0	300	400	V	
VD	Control supply voltage	Applied between VP1-VNC, VN1-VNC	13.5	15.0	16.5	V	
VDB	Control supply voltage	Applied between VUFB-U, VVFB-V, VWFB-W	13.0	15.0	18.5	V	
ΔVD, ΔVDB	Control supply variation		-1	—	1	V/μs	
tdead	Arm shoot-through blocking time	For each input signal, Tc ≤ 100°C	1.5	—	—	μs	
fPWM	PWM input frequency	Tc ≤ 100°C, Tj ≤ 125°C	—	—	20	kHz	
Io	Allowable r.m.s. current	VCC = 300V, VD = VDB = 15V, P.F = 0.8, sinusoidal PWM, Tj ≤ 125°C, Tc ≤ 100°C (Note 9)	fPWM = 5kHz	—	—	4.0	Arms
			fPWM = 15kHz	—	—	2.5	
PWIN(on)	Allowable minimum input pulse width	(Note 10)	0.5	—	—	μs	
PWIN(off)			0.5	—	—		
VNC	VNC variation	Between VNC-N (including surge)	-5.0	—	5.0	V	

Note 9: The allowable r.m.s. current value depends on the actual application conditions.

10: IPM might not make response if the input signal pulse width is less than the recommended minimum value.

Fig. 7 THE DIP-IPM INTERNAL CIRCUIT



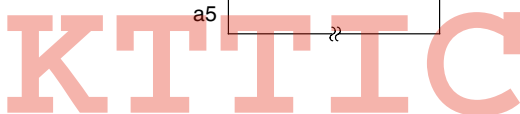
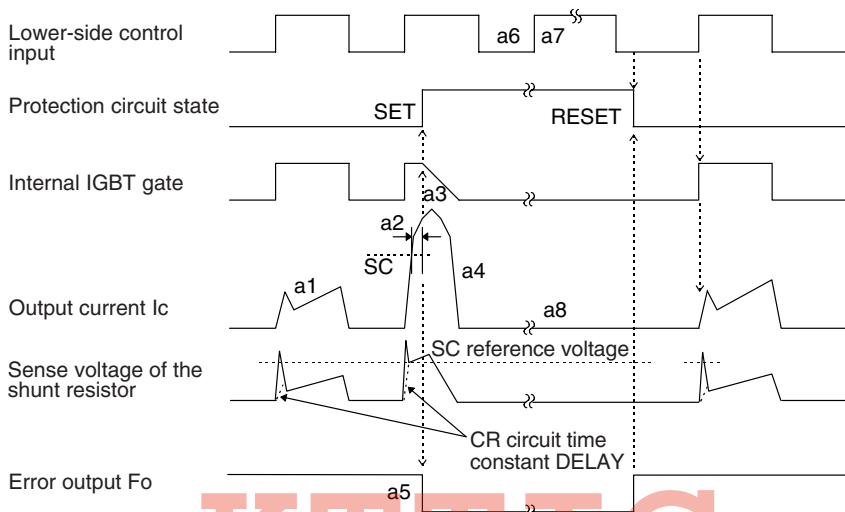
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TRANSFER-MOLD TYPE
INSULATED TYPE

Fig. 8 TIMING CHART OF THE DIP-IPM PROTECTIVE FUNCTIONS

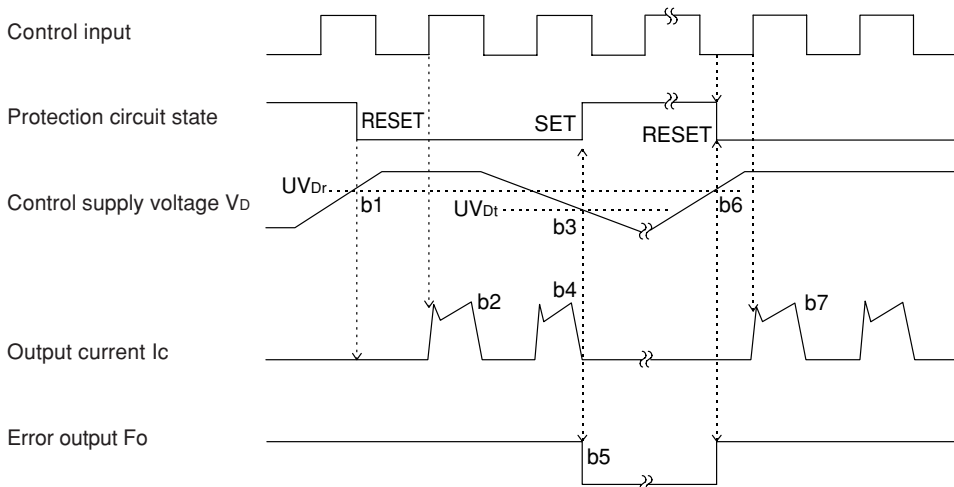
[A] Short-Circuit Protection (Lower-side only with the external shunt resistor and CR filter)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit detection (SC trigger).
- a3. IGBT gate hard interruption.
- a4. IGBT turns OFF.
- a5. Fo outputs ($t_{FO(min)} = 20\mu s$).
- a6. Input "L" : IGBT OFF.
- a7. Input "H" : IGBT ON.
- a8. IGBT OFF in spite of input "H".



[B] Under-Voltage Protection (Lower-side, UV_D)

- b1. Control supply voltage rising : After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV_{Dt}).
- b4. IGBT OFF in spite of control input condition.
- b5. Fo outputs ($t_{FO} \geq 20\mu s$ and Fo outputs continuously during UV period).
- b6. Under voltage reset (UV_{Dr}).
- b7. Normal operation : IGBT ON and carrying current.

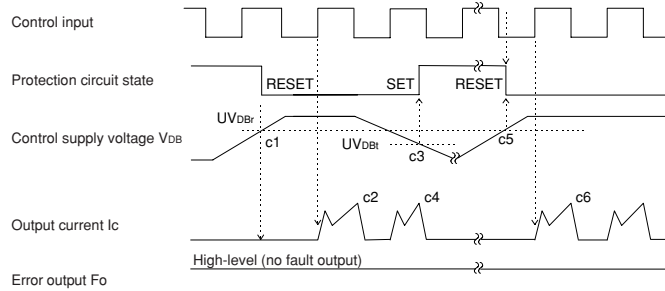


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TRANSFER-MOLD TYPE
INSULATED TYPE

[C] Under-Voltage Protection (Upper-side, UVDB)

- c1. Control supply voltage rising : After the voltage level reaches UVDBr, the circuits start to operate when next input is applied.
- c2. Normal operation : IGBT ON and carrying current.
- c3. Under voltage trip (UVDBt).
- c4. IGBT OFF in spite of control input signal level, but there is no Fo signal outputs.
- c5. Under voltage reset (UVDBr).
- c6. Normal operation : IGBT ON and carrying current.



[D] Over Temperature Protection (Lower-side, OT)

- d1. Normal operation : IGBT ON and carrying current.
- d2. LVIC temperature exceeds over temperature trip level (OTt).
- d3. IGBT OFF in spite of control input condition.
- d4. Fo outputs during over temperature period, however, the minimum pulse width is 20µs.
- d5. LVIC temperature becomes under over temperature reset level.
- d6. Circuits start to operate normally when next input is applied.

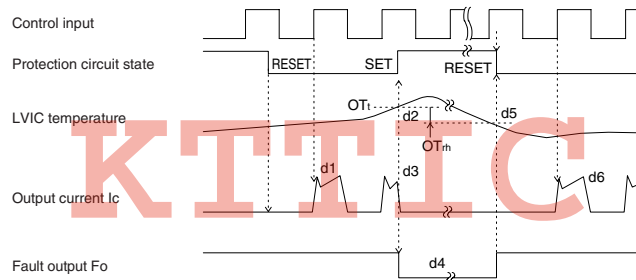
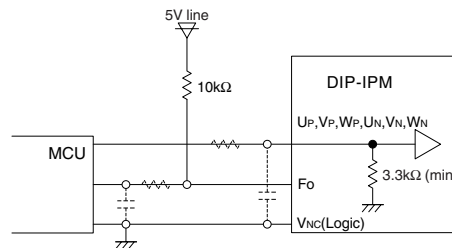
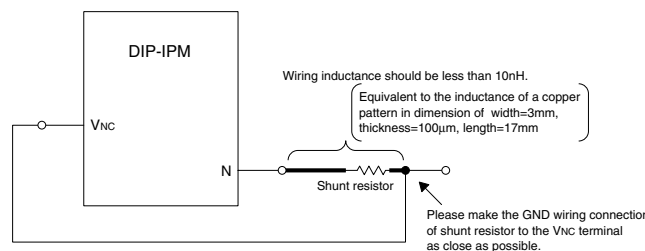


Fig. 9 RECOMMENDED MCU I/O INTERFACE CIRCUIT



Note : The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.
The DIP-IPM input section integrates a 3.3kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

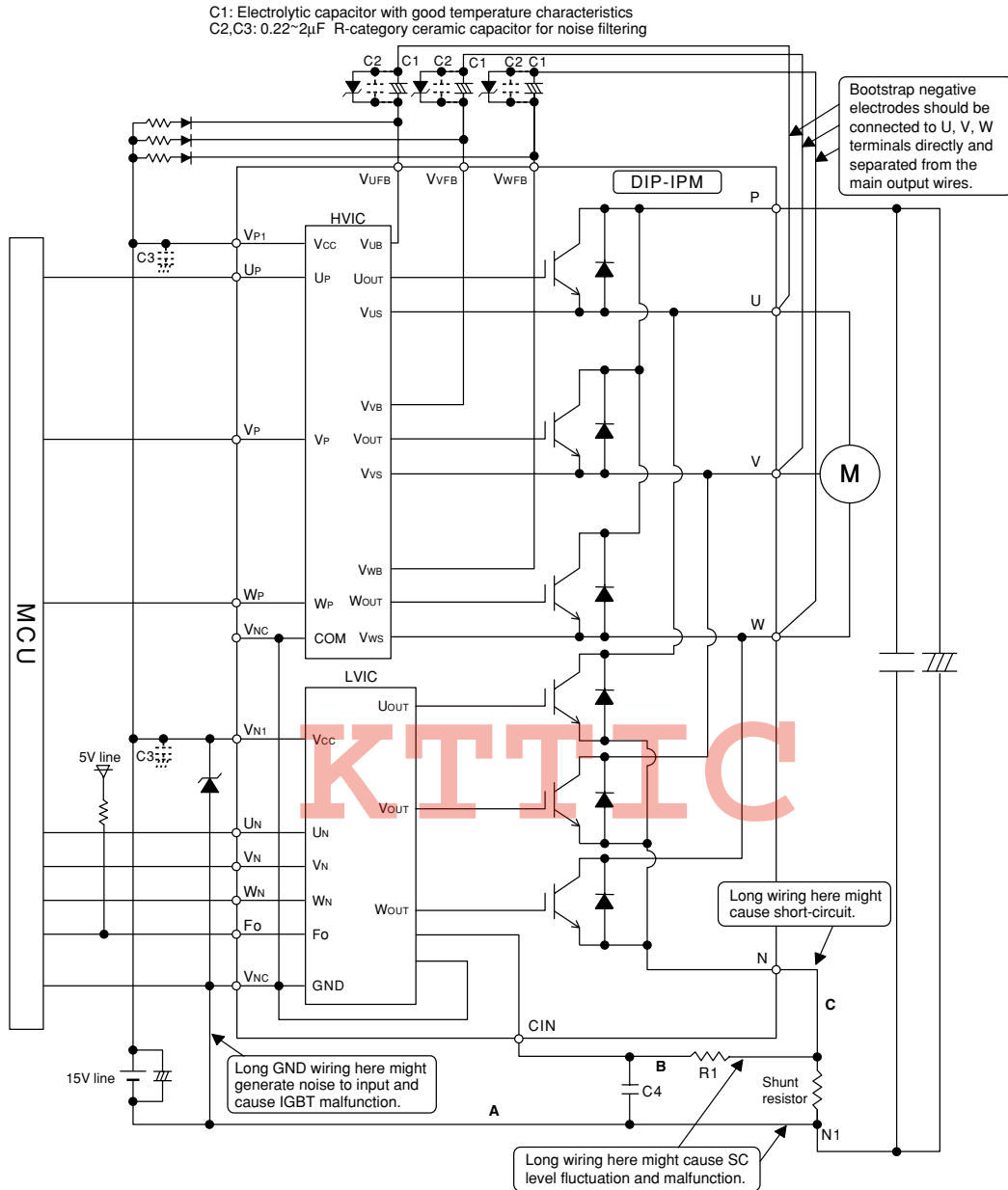
Fig. 10 WIRING CONNECTION OF SHUNT RESISTOR



PS21963-ET/-AET/-CET/-ETW

TRANSFER-MOLD TYPE
INSULATED TYPE

Fig. 11 AN EXAMPLE OF TYPICAL DIP-IPM APPLICATION CIRCUIT



- Note 1** : Input drive is High-Active type. There is a 3.3kΩ(min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
- 2** : Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
- 3** : Fo output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.
- 4** : To prevent erroneous protection, the wiring of A, B, C should be as short as possible.
- 5** : The time constant R1C4 of the protection circuit should be selected in the range of 1.5~2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1, C4.
- 6** : All capacitors should be mounted as close to the terminals of the DIP-IPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2, C3: good temperature, frequency and DC bias characteristic ceramic type are recommended.)
- 7** : To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber between the P-N1 terminals is recommended.
- 8** : Two Vnc terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.
- 9** : It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
- 10** : If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point.