HongKong HK12B5

SEMICONDUCTOR **16M×8 Nonvolatile SRAM**

FEATURES

- ►Data retention in the SRAM when absence of Vcc
- ►Data is automatically protected during power loss
- ►Directly replaces 16M×8 volatile static RAM or EEPROM
- ►Unlimited write cycles
- ►Low-power CMOS operation
- ►Over 10 years of data retention
- ►Standard 40-pin JEDEC pinout
- ►Available in 70,85,100 ns access times
- ►Read cycle time equals write cycle time
- ►Optional ±5% and ±10% operating range
- ►Optional industrial temperature range of -40°C to +70°C, designated IND

PIN ASSIGNMENT

NC	1	40	Vcc
NC	2	39	A23
A20	3	38	V_{CC}
A19	4	37	A21
A18	5	36	A22
A16	6	35	A15
A14	7	34	A17
A12	8	33	WE
A7	9	32	A13
A6	10	31	A8
A5	11	30	A9
A4	12	29	A11
A3	13	28	OE
A2	14	27	A10
A1	15	26	CE
A0	16	25	DQ7
DQ0	17	24	DQ6
DQ1	18	23	DQ5
DQ2	19	22	DQ4
GND	20	21	DQ3

PIN DESCRIPTION

A0-A23	Address Inputs
CE	Chip Enable（Low Enable）
GND	Ground
DQ0-DQ7	Data In/Data Out
Vcc	Power (+5V)
WE	Write Enable（Low Enable）
OE	Output Enable（Low Enable）
NC	No Connect

DESCRIPTION

The HK12B5 131072k Nonvolatile SRAM is 134,217,728-bit, fully static, nonvolatile SRAM organized as 16M words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors Vcc for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switches on and writes protection is unconditionally enabled to prevent garbled. The NV SRAM can be used in place of existing 16M×8 static RAMs directly conforming to the popular byte wide 40 pin DIP standard. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

OPERATION

Read Mode

The HK12B5 executes a read cycle whenever WE (Write Enable) is inactive (high) andCE

(Chip Enable) is active (low). The unique address specified by the 24 address inputs(A_0-A_{23}) defines which of the 134,217,728 bytes of data is to be accessed. Valid data willbe available to the eight data output drivers within t_{ACC}(Access time) after the last addressInput signal is stable, providing that CE and OE (Output Enable) access times are alsosatisfied. If OE and CE access times are not satisfied, then data access must be measured form the later occurring signal (CE or OE) and the limiting parameter is either t_{CO} for CEor t_{OE} for OE rather than address access.

Write Mode

The HK12B5 is in the write mode whenever the CE signals and WE are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enable (CE and OE active) then WE will disable the outputs in t_{ODW} from its falling edge.

Date Retention Mode

The HK12B5 provides full functional capability for V_{CC} greater than 4.5 or 4.75 volts and write protects by 4.35 or 4.75 volts. Date is maintained in the absence of $V_{CC,}$ without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. While the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become“don’t care” and all outputs are high impedance. As Vcc falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when Vcc rises above approximately 3.0 volts, the power switching circuit connects external Vcc to the RAM. Normal RAM operation can resume after Vcc exceeds 4.5 or 4.75 volts for HK12B5.

SEAL AND SHIPPING

The HK12B5 is shipping from HK semiconductor with the lithium energy source connected. But we guaranteed the energy capacity will not less than 90% full energy capacity. Normally, we supply full energy capacity chips to you.

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relation to Ground	-0.3V to +6.0V
Operating Temperature	0°C to 70°, -40° to +70°C for IND parts
Storage Temperature	-40°C to +70°C, -40°C to+70°C for IND parts
Soldering Temperature	200°C for 3 seconds

This is stress rating only functional operation of the device at these or any other conditions above those indicated in the operation sections of the specification is not implied. Exposure to absolute maximum rating conditions for long of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°Cto70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage 1（HK12B5）	V_{cc}	4.5	5.0	5.5	V
Power Supply Voltage 1（HK12B5N）	V_{cc}	4.75	5.0	5.5	V
Logic1	V_{IH}	2.2	—	Vcc	V
Logic0	V_{IL}	0.0	—	+0.8	V

DC ELECTRICAL CHARACTERISTICS (0°Cto70°C; Vcc=5V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	-5.0	—	+ 5.0	mA
I/O Leakage Current CE≤V_{IH}≤Vcc	I_{IO}	-5.0	—	+ 5.0	mA

Output Current @2.4V	I_{OH}	-1.0	—	—	mA
Output Current @0.4V	I_{OL}	2.0	—	—	mA
Standby Current CE=2.2V	I_{CCS1}	—	5.0	10.0	mA
Standby Current CE=Vcc-0.5V	I_{CCS2}	—	3.0	5.0	mA
Operating Current	I_{CCO1}	—	5	85	mA
Write Protection Voltage 1（HK12B5）	V_{TP}	4.25	4.37	4.5	V
Write Protection Voltage 2（HK12B5N）	V_{TP}	4.5	4.75	4.85	V

CAPACITANCE

PARAMETER	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C_{IN}	5	10	pF
Input/output Capacitance	$C_{I/O}$	5	12	pF

AC ELECTRICAL CHARACTERI STICS (0°Cto70°C;Vcc=5V±10%)

PARAMETER	SYM	HK12B5-70		HK12B5-85		HK12B5-100		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70	—	85	—	100	—	ns	—
Access Time	t_{ACC}	—	70	—	85	—	100	ns	—
OE to Output Valid	t_{OE}	—	35	—	45	—	50	ns	—
OE To Output Valid	t_{CO}	—	70	—	85	—	100	ns	—
OE or CE to Output	t_{COE}	5	—	5	—	5	—	ns	5
Output High Z from Dissection	t_{OD}	—	25	—	30	—	35	ns	5
Output Hold from Address change	t_{OH}	5	—	5	—	5	—	ns	—
Write Cycle Time	t_{WC}	70	—	85	—	100	—	ns	
Write Pulse Width	t_{WP}	55	—	65	—	75	—	ns	3
Address Setup Time	t_{AW}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15	—	5 15	—	5 15	—	ns	
Output High Z From	t_{ODW}	—	25	—	30	—	35	ns	5
Output Active from	t_{OEW}	5	—	5	—	5	—	ns	5
Data Setup Time	t_{DS}	30	—	35	—	40	—	ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10	—	0 10	—	0 10	—	ns	

The parameter above all are designed data, please prolong more times for write operation because the cycle time maybe delay by the protect circuitry.

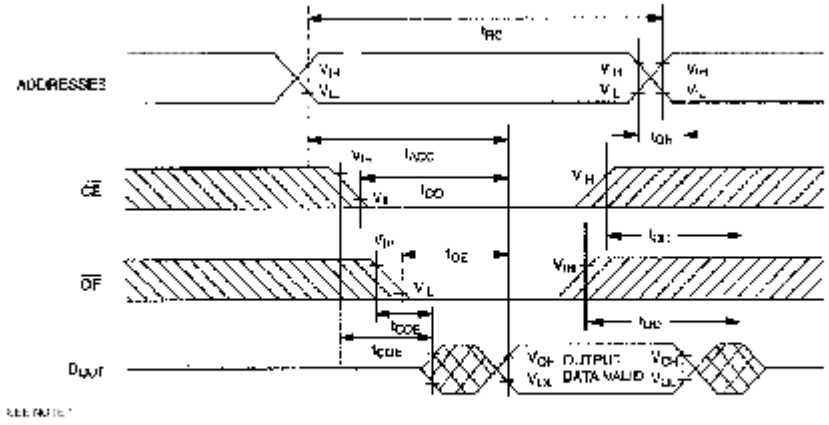
POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE at VIH before Power-Down	20	—	μs	—
t_F	V_{CC} Slew from 4.5V to 0V(CE at VIH)	300	—	μs	—
t_R	V_{CC} Slew from 0V to 4.5V(CE at VIH)	0	—	μs	—
t_{REC}	CE WE at VIH after Power-UP	2	125	ms	—

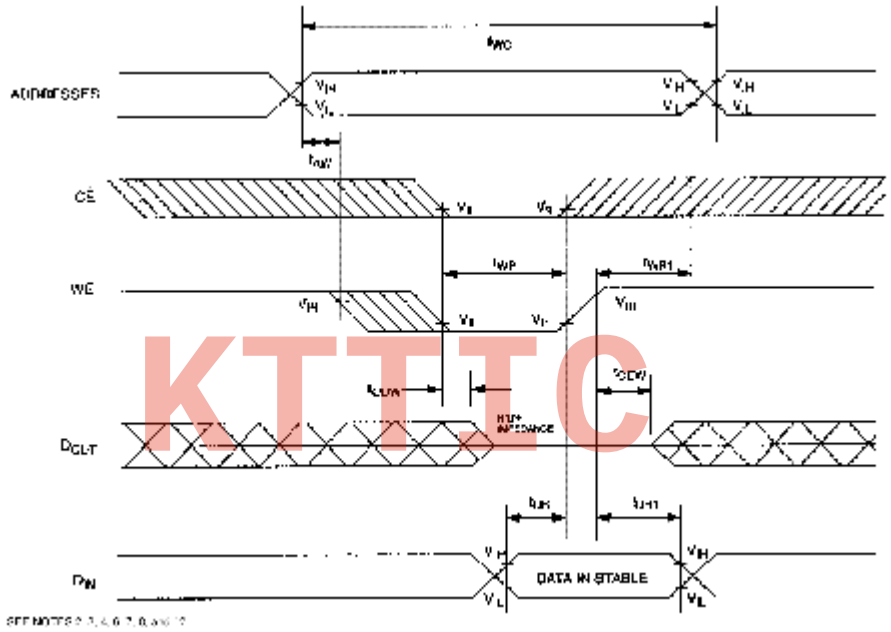
(t_A=25°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	—	10	—	years	9,10

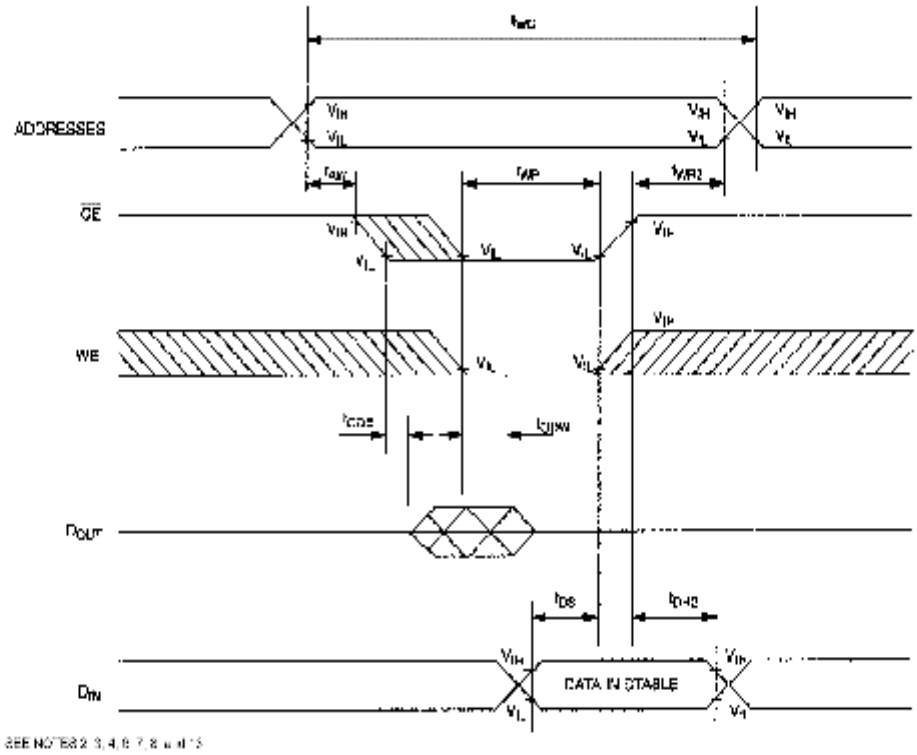
READ CYCLE



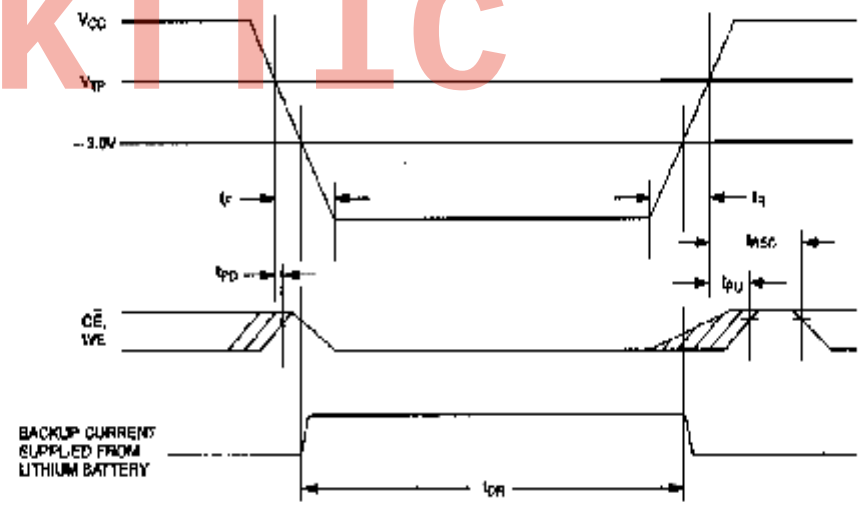
WRITE CYCLE 1



WRITE CYCLE 2



POWER-DOWN/POWER-UP CONDITION



WARNING:

Under no circumstances are negation undershoots, of any amplitude, allowed when

device is in the battery backup mode.

NOTE:

1. WE is high for a Read Cycle
2. OE= V_{IH} or $V_{IL.}$ If OE= V_{IH} during write cycle, the output butters remain in a high impedance state.
3. t_{WP} is specified as the logical AND of CE and WE . T_{WP} is measured from the latter of CE or WE going low to the earlier of CE or WE going high.
4. $t_{DH,}$ t_{DS} are measured from the earlier of CE or WE going high.
5. These parameters are sampled with a 5pF load and are not 100% tested.
6. If the CE low transition occurs simultaneously with or latter than the WE low transition in Write Cycle1, the output buffers remain in a high impedance state during this period.
7. If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in high impedance state during this period.
8. If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition the output buffers remain in a high impedance state during this period.
9. All DC operating conditions DC electrical characteristics and Ac electrical characteristics apply to both standard part and those designated IND Parts with the IND designated meet specifications over a temperature of -40°C to+70°C.
10. The expected date retention time is under the specified condition (at 25°C). If the IC is exposed continuously to the max test condition and max temperatures, the life of the IC will be shorted. In a power down condition the voltage on any pin may not exceed the voltage on Vcc.
11. In a power down condition the voltage on any pin may not exceed the voltage on Vcc.
12. t_{WR1}, t_{DH1} are measured from WE going high.
13. t_{WR2}, t_{DH2} are measured from CE going high.

DC TEST CONDITION

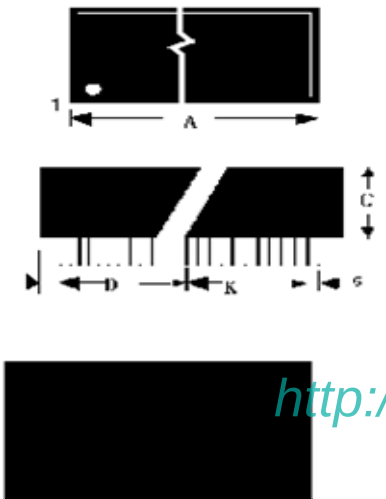
Outputs Open
Cycle=200ns for operating current
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100pF+1TTL Gate
Input Pulse Levels: 0-3.0V
Timing Measurement Reference Levels
Input:
1.5V Output:
1.5V
Input pulse Rise and Fall Times: 5ns

HK12B5 NONVOLATILE SRAM 40 PIN 740 MILMODULE

PKG	40-PIN	
DIM	MIN	MAX
A IN	2.118	2.137
MM	53.80	54.30
B IN	0.720	0.740
MM	18.29	18.80
C IN	0.571	0.591
MM	14.52	15.02
D IN	0.080	0.110
MM	2.03	2.79
G IN	0.090	0.110
MM	2.29	2.79
H IN	0.590	0.630
MM	14.99	16.00



J IN MM	0.008 0.20	0.012 0.30
K IM MM	0.015 0.38	0.021 0.53