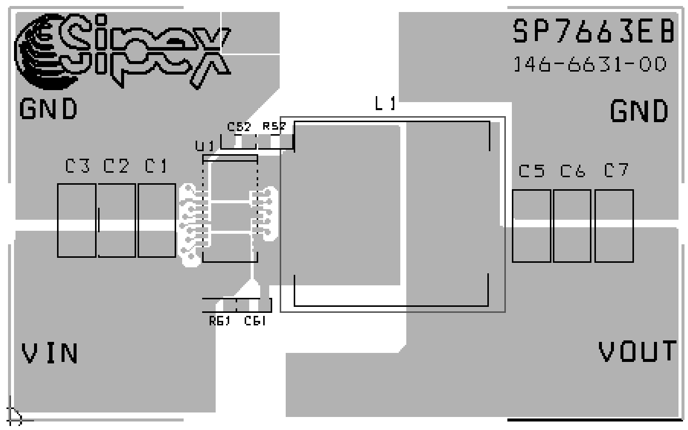
Solved by Sipex

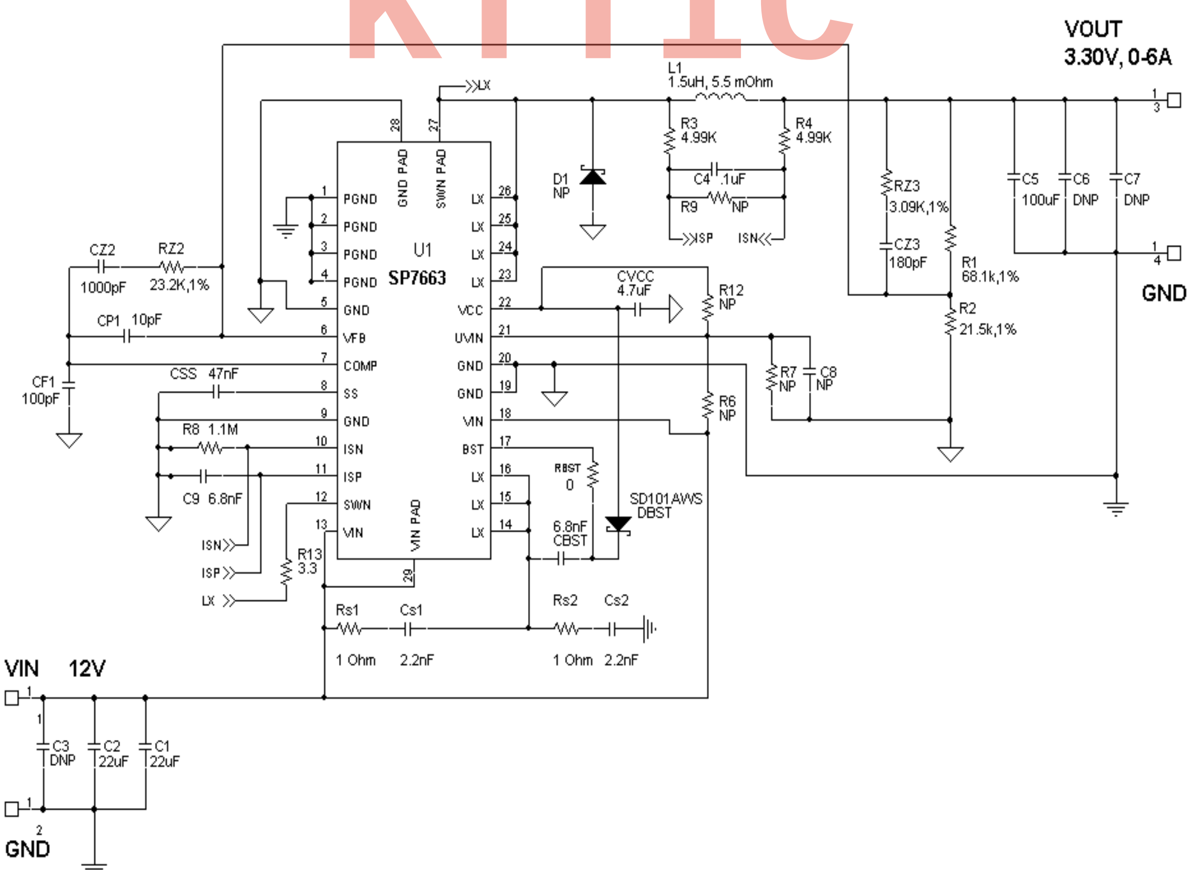
SP7663

Evaluation Board Manual

- Easy Evaluation for the SP7663ER 0 to 22V Input, 0 to 6A Output Synchronous Buck Converter
- Built-in low RDS(ON) Power FETs
- UVLO Detects Both VCC and VIN
- High Integrated Design, Minimal Components
- High Efficiency: 90%
- Feature Rich: UVIN, Programmable Soft Start, Built-in VCC Supply, Current Limiting and Output Short Circuit Protection



SP7663EB SCHEMATIC



1) Powering Up the SP7663EB Circuit
Connect the SP7663 Evaluation Board with an external +12V power supply. Connect with short leads and large diameter wire directly to the "VIN" and "GND2" posts. Connect a Load between the VOUT and GND1 posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics
It's best to GND reference all scope and digital meters using the Star GND post in the center of the board. VOUT ripple can best be seen by touching the probe tip to the pad for C3 and the scope to the GND collar touching Star GND post – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages
While the SP7663 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP7663 can be set to other output voltages. The relationship in Equation 1 is based on a voltage divider from the output to the feedback pin V_{FB}, which is set to an internal reference voltage of 0.80V. Note, due to the common mode voltage range of the current sense amplifier, output voltages greater than 3.3V are only possible if the current sense is disabled. To disable current limit, remove R3 and R4. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$R2 = \frac{R1}{\left(\frac{VOUT}{.80V} - 1\right)} \quad \text{Equation1}$$

Where R1 = 68.1KΩ and for V_{OUT} = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of the R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that 50KΩ ≤ R1 ≤ 100KΩ for overall system loop stability.

Note that since the SP7663 Evaluation Board design was optimized for 12V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section. In addition, the SP7663ER provides short circuit protection by sensing V_{OUT} at GND. The current limit of the converter is set to about 9A which is accomplished by sensing the current through the inductor. To adjust the current limit, follow Equations 2 and 3 to set the current limit accordingly. The current limit should be set to about 50% higher than the maximum output current that is desired. This will prevent the part from accidentally triggering the current limit during large transient load steps.

Adjusting the current upwards is done by adjusting resistor R9.

$$R9 = \frac{60mV \bullet (R3 + R4)}{I\max \bullet (DCR - 60mV)} \quad \text{Equation 2}$$

Where: DCR is the Inductor winding resistance
I_{MAX} is the desired output current

Adjusting the current downwards is controlled by adjusting R8.

$$R8 = R4 \cdot \left(\frac{(Vout - 60mV) + (Imax \bullet DCR)}{60mV - (Imax \bullet DCR)} \right) \quad \text{Equation 3}$$

Where: DCR is the Inductor winding resistance
IMAX is the desired output current

Further details on the current limit can be found in the SP7663 data sheet.

POWER SUPPLY DATA

The SP7663ER is designed with an accurate 2.0% reference over line, load and temperature. Figure 1 data shows a typical SP7663 evaluation board efficiency plot, with efficiencies up to 90% and output currents up to 6A. The output voltage ripple of less than 50mV at full load and the LX node are shown in figure 2. Figures 3 and 4 illustrate a 3A-to-6A and 0A-to-6A Load Step. Short circuit and current limit are shown in Figures 5 and 6. Typical startup characteristics into a full load and no load are shown in figure 7 and 8. All data was taken at $12V_{IN}$.

While data on individual power supply boards may vary, the capability of the SP7663ER of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

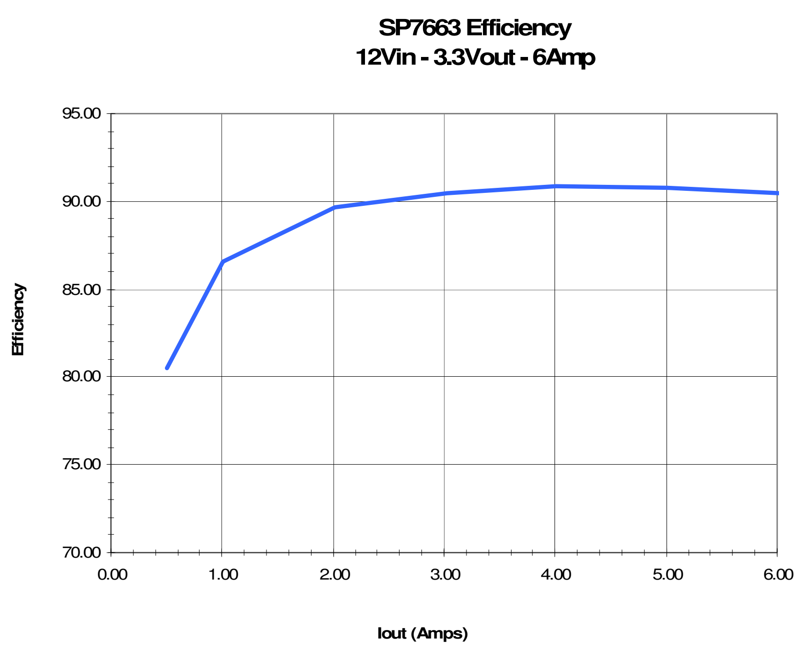


Figure 1. Efficiency vs. Load

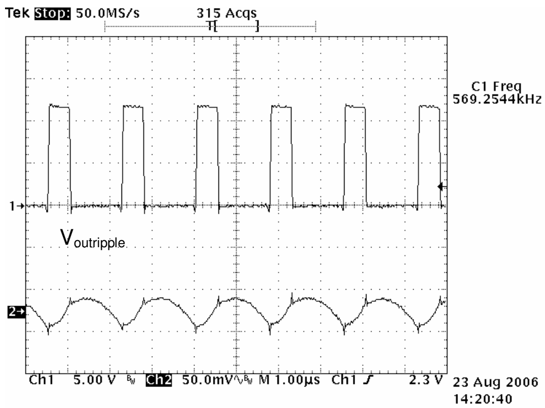


Figure 2. LX node output ripple voltage

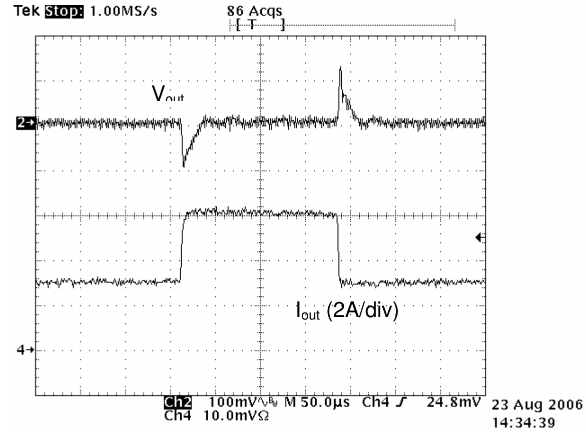


Figure 3. Load Step Response: 3->6A

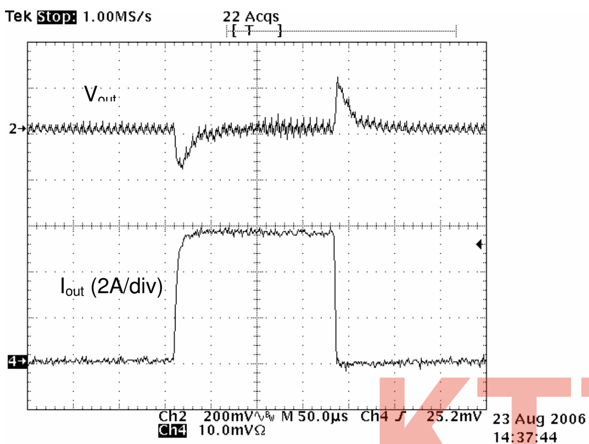


Figure 4. Load Step Response 0->6A

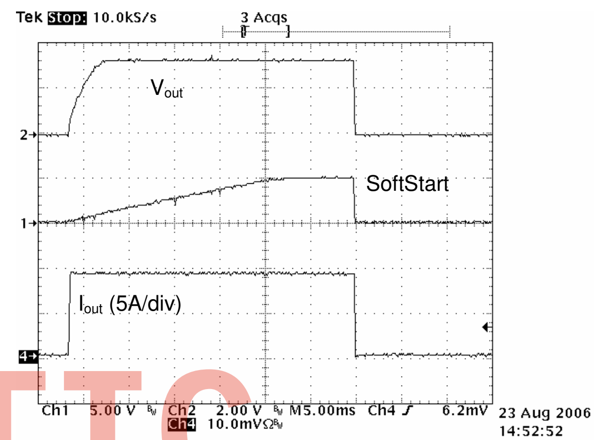


Figure 5. Current Limit set point 9A

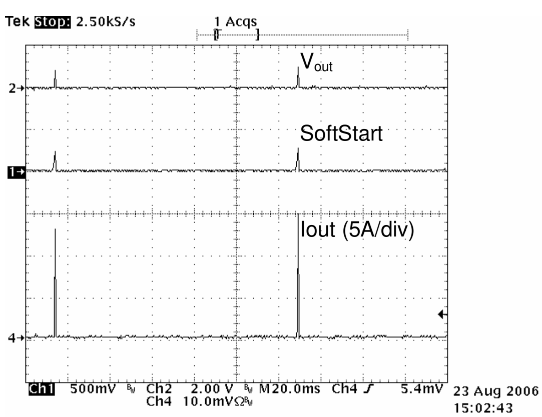


Figure 6. Output load Short Circuit

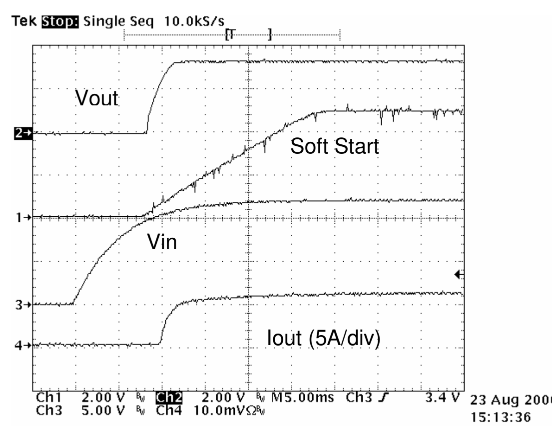


Figure 7. Startup into full load

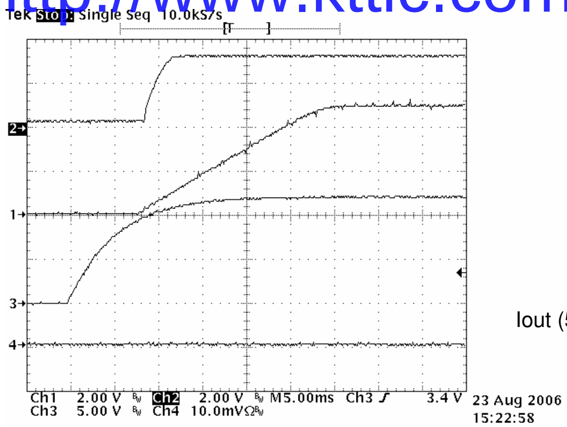


Figure 8. Startup into no load

TYPE III LOOP COMPENSATION DESIGN

The open loop gain of the SP7663EB can be divided into the gain of the error amplifier **Gamp(s)**, PWM modulator **Gpwm**, buck converter output stage **Gout(s)**, and feedback resistor divider **Gfbk**. In order to cross over at the selecting frequency **fco**, the gain of the error amplifier must compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec. The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 to 1/10 of the switching frequency **fs** to insure proper operation. Since the SP7663EB is designed with Ceramic Type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** underdamped resonance double pole frequency.

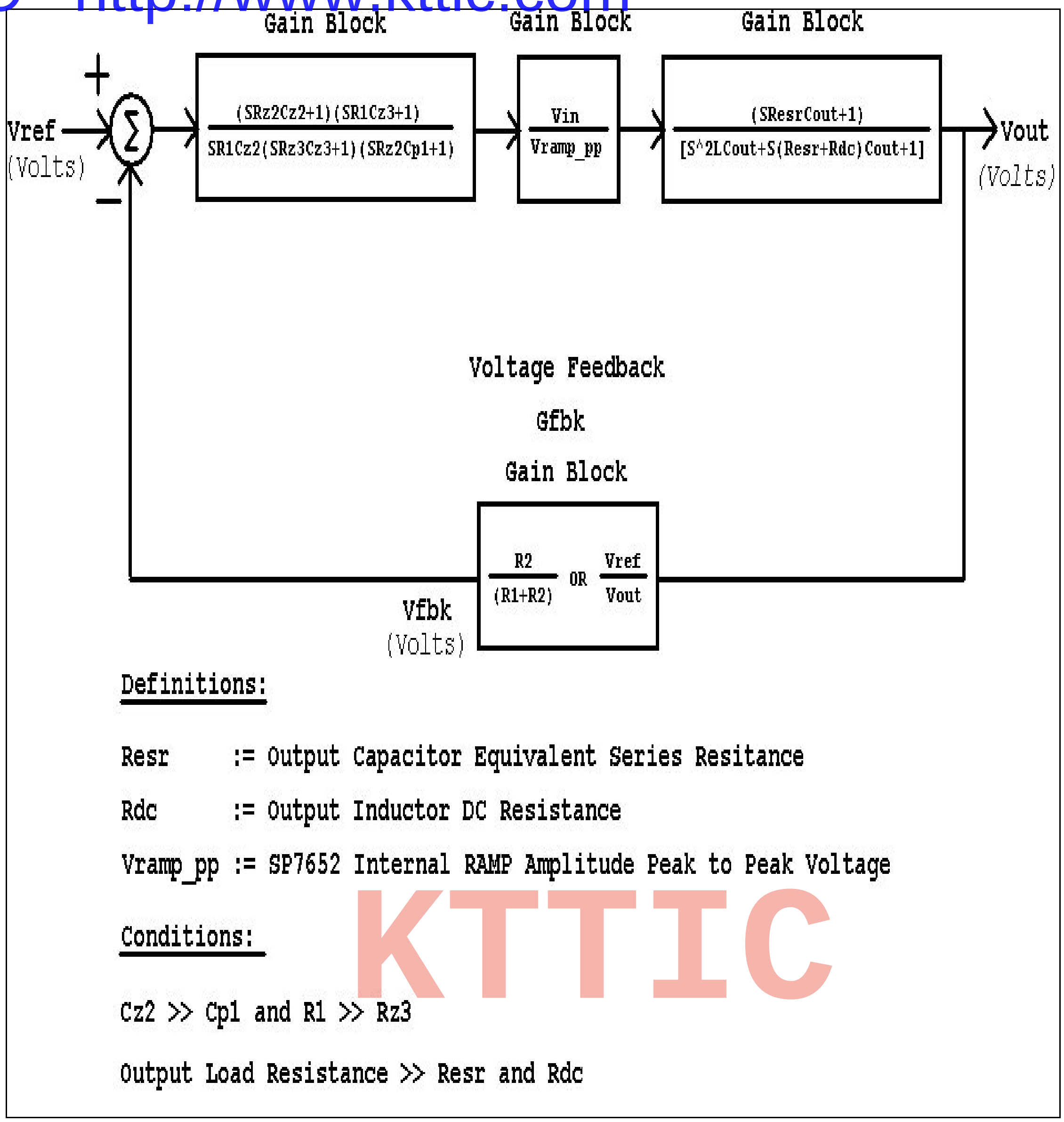


Figure 9. Voltage Mode Control Loop with Loop Dynamic for Type III Compensation

The simple guidelines for positioning the poles and zeros and for calculating the component values for Type III compensation are as follows. As a particular example, consider for the following SP7663EB with a **Type III** Voltage Loop Compensation component selections:

Input requirements and inductor selection

Vin = 5 to 13.5V
Vout = 3.30V @ 0 to 6A load
Select **L = 1.5uH** => yield ≈ 48% of maximum 6A output current ripple.
Select **Cout = 100uF Ceramic** capacitor (RESR ≈ **4mΩ**)
fs = 600kHz SP7663 internal Oscillator Frequency
VRAMP_PP = 1.0V SP7663 internal Ramp Peak-to-Peak Amplitude

Step by step design procedures:

Note: Loop Compensation component calculations discussed in this section are further elaborated in the application note #ANP16, "**Loop Compensation of Voltage-Mode Buck Converters".**

These calculations shown here can be quickly iterated with the Type III Loop Compensation Calculator on the web at: www.sipex.com/files/Application-Notes/TypeIIICalculator.xls

Choose $\text{fco} = \text{fs}/10$

$$\text{fco} = 600\text{Khz}/10 = 60\text{Khz}$$

Calculate **fp_LC,** the double pole frequency of the filter

$$\text{fp\_LC} = \frac{1}{2\pi(\sqrt{\text{L}\cdot\text{C}})}$$

$$\text{fp\_LC} = \frac{1}{2\pi\cdot\sqrt{1.5uH\cdot 100uF})} = 12.99Khz \approx 13\text{Khz}$$

Calculate **fz_ESR** the ESR zero frequency

$$\text{fz\_ESR} = \frac{1}{2\pi\cdot\text{Cesr}\cdot\text{Cout}}$$

$$fz\_ESR = \frac{1}{2\pi\cdot(4m\Omega)\cdot(100\mu F)} = 397.88Khz \approx 400\text{K}hz$$

Select **R1** component value such that 50kΩ ≤ R1 ≤ 100kΩ
R1 = 68.1kΩ, 1%

Calculate **R2** base on the desired VOUT

$$R2 = \frac{R1}{\left[\frac{Vout}{.8V}\right]-1}$$

$$R2 = \frac{68.1K\Omega}{\left[\frac{3.3V}{.8V}\right]-1} = 21.79K\Omega \approx 21.5K\Omega$$

Select the ratio of **RZ2** / **R1** gain for the desired gain bandwidth

$$RZ2 = R1\cdot\left[\frac{Vramp\_pp}{Vin\_\text{max}}\right]\cdot\left(\frac{fco}{fp\_LC}\right)$$

$$RZ2 = R1\cdot\left[\frac{1V}{13.5V}\right]\cdot\left(\frac{60KHz}{13KHz}\right) = 23.2K\Omega$$

Calculate **CZ2** by placing the zero at ½ of the output filter pole frequency

$$CZ2 = \frac{1}{\pi \cdot RZ2 \cdot fp\_LC}$$

$$CZ2 = \frac{1}{\pi \cdot 23.2K\Omega \cdot 13KHz} = 1.055nF \approx 1nF$$

Calculate **CP1** by placing the first pole at ESR zero frequency

$$CP1 = \frac{1}{2\pi \cdot (Rz2 \cdot fz\_ESR)}$$

$$CP1 = \frac{1}{2\pi \cdot (68.1K \cdot 400KHz)} = 5.84pF \approx 10pF$$

Calculate **RZ3** by setting the second pole at ½ of the switching frequency and the second zero at the output filter double pole frequency

$$RZ3 = \frac{2 \cdot (R1) \cdot (fp\_LC)}{fs - 2fp\_LC}$$

$$RZ3 = \frac{2 \cdot (68.1K\Omega) \cdot (13KHz)}{600KHz - 2f13KHz} = 3.084K\Omega$$

Calculate **CZ3** from **RZ3** component value above

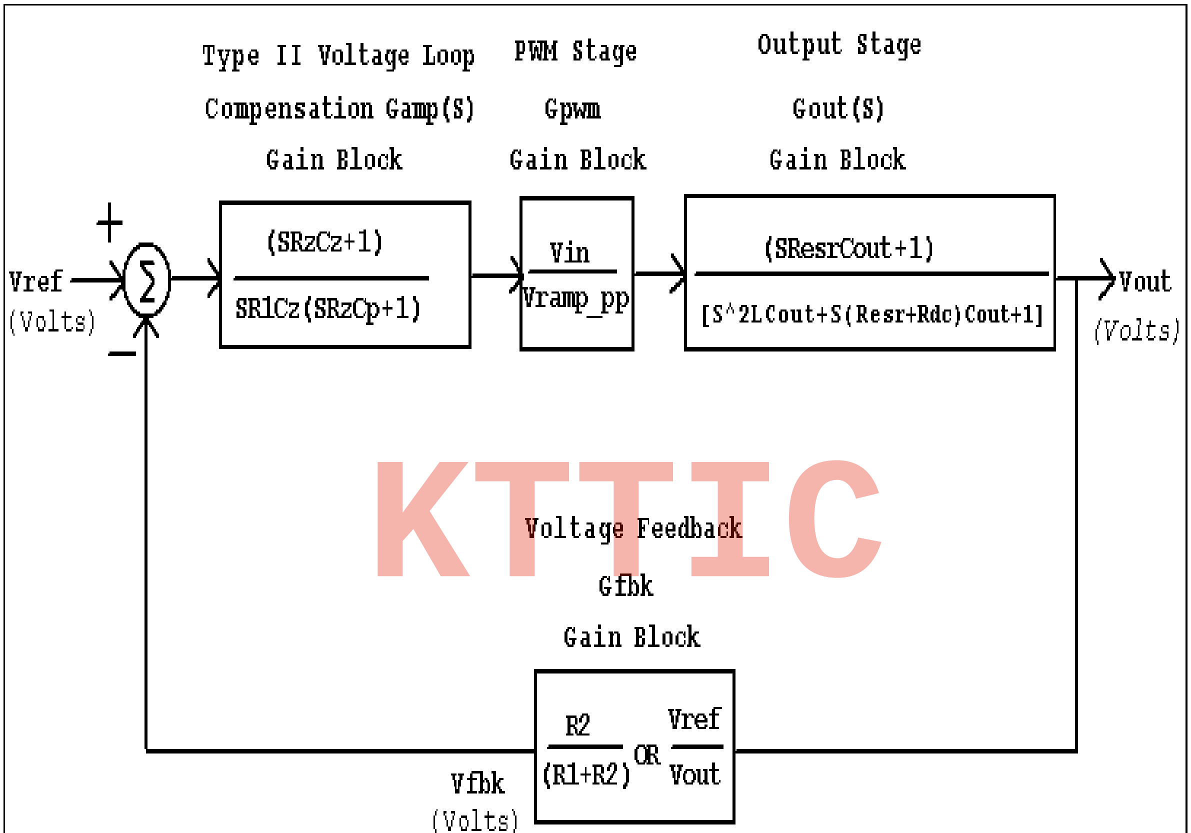
$$CZ3 = \frac{1}{\pi \cdot RZ3 \cdot fs}$$

$$CZ3 = \frac{1}{\pi \cdot 3.084K\Omega \cdot 600KHz} = 172pF \approx 180pF$$

Choose 100pF ≤ **CF1** ≤ 220pF to stabilize the SP7663ER internal Error Amplifier

TYPE II LOOP COMPENSATION DESIGN

Type II compensation is specifically used when an Electrolytic or Tantalum output capacitor is chosen at the converter output due to its low cost. In that case, the zero caused by the output capacitor ESR is within a few kHz and this is of course greatly simplifying the voltage loop compensation design. By adding an additional zero in the compensation loop before the first pole, the voltage loop bandwidth is extended with a 90º phase boost and hence the overall transient response time is improved. Most previous guidelines for calculating the component values for Type III compensation can be carries over for Type II except for the new **Rz**, **Cz** and **Cp** components. Note that RZ2, CZ2, CP1, RZ3, and CZ3 components are not required for the Type II Loop Compensation Design.



Definitions:

Resr := Output Capacitor Equivalent Series Resitance

Rdc := Output Inductor DC Resistance

Vramp_pp := SP7652 Internal RAMP Amplitude Peak to Peak Voltage

Conditions:

Cz >> Cp

Output Load Resistance >> Resr and Rdc

Figure 10. Voltage Mode Control Loop with Loop Dynamic for Type II Compensation

As a particular example, consider for the following SP7663EB with a **Type II** Voltage Loop Compensation component selections:

Input requirements and inductor selection
Vin = 5 to 13.5V
Vout = 3.30V @ 0 to 6A load
Select **L = 1.5uH** => yield ≈ 48% of maximum 6A output current ripple.
Select **COUT = 330uF Tantalum** capacitor (RESR ≈ **35mΩ**)
fs = 600kHz SP7663 Internal Oscillator Frequency
VRAMP_PP = 1.0V SP7663 internal Ramp Peak-to-Peak Amplitude

Step-by-step design procedures:

> Note: Type II Loop Compensation component calculations discussed in this section are further elaborated in the application note #ANP18, "**Selecting Appropriate Compensation: Type-II or Type-III**".
>
> These calculations shown here can be quickly iterated with the Type III Loop Compensation Calculator on the web at:
> http://www.sipex.com/files/ApplicationNotes/Copy%20of%20Type%20II%20calculator5.xls

Choose

$$\text{fco} = \text{fs}/10$$

$$\text{fco} = 600\text{Khz}/10 = 60\text{Khz}$$

Calculate **fp_LC,** the double pole frequency of the filter

$$\text{fp\_LC} = \frac{1}{2\pi(\sqrt{\text{L} \cdot \text{C}})}$$

$$\text{fp\_LC} = \frac{1}{2\pi \cdot \sqrt{1.5uH \cdot 330uF}} = 7.153Khz \approx 7.2\text{Khz}$$

Calculate **fz_ESR,** the ESR zero frequency

$$\text{fz\_ESR} = \frac{1}{2\pi \cdot \text{Cesr} \cdot \text{Cout}}$$

$$fz\_ESR = \frac{1}{2\pi \cdot (35m\Omega) \cdot (330\mu F)} = 13.77Khz \approx 14\text{K}hz$$

Select **R1** component value such that 50kΩ ≤ R1 ≤ 100kΩ
R1 = 68.1kΩ, 1%

Calculate **R2** base on the desired VOUT

$$R2 = \frac{R1}{\left[\frac{Vout}{.8V}\right] - 1}$$

$$R2 = \frac{68.1K\Omega}{\left[\frac{3.3V}{.8V}\right] - 1} = 21.79K\Omega \approx 21.5K\Omega$$

Select the ratio of **RZ2** / **R1** gain for the desired gain bandwidth

$$RZ2 = R1 \cdot \left(\frac{Vramp\_pp}{Vin\_\max}\right) \cdot \left(\frac{Fz\_ESR}{(Fp\_LC)^2}\right) \cdot fco$$

$$RZ2 = 68.1K\Omega \cdot \left(\frac{1}{13.5V}\right) \cdot \left(\frac{13Khz}{7.2Khz^2}\right) \cdot 60Khz = 75.89K\Omega \approx 75K\Omega$$

Calculate **CZ2** by placing the zero at 1/10 of the output filter pole frequency

$$CZ2 = \frac{1}{.1 \cdot 2 \cdot \pi \cdot RZ2 \cdot fp\_LC}$$

$$CZ2 = \frac{1}{.1 \cdot 2 \cdot \pi \cdot 75K\Omega \cdot 7.2Khz} = 294pF \approx 330pF$$

Calculate **CP1** by placing the second pole at ½ of the switching frequency

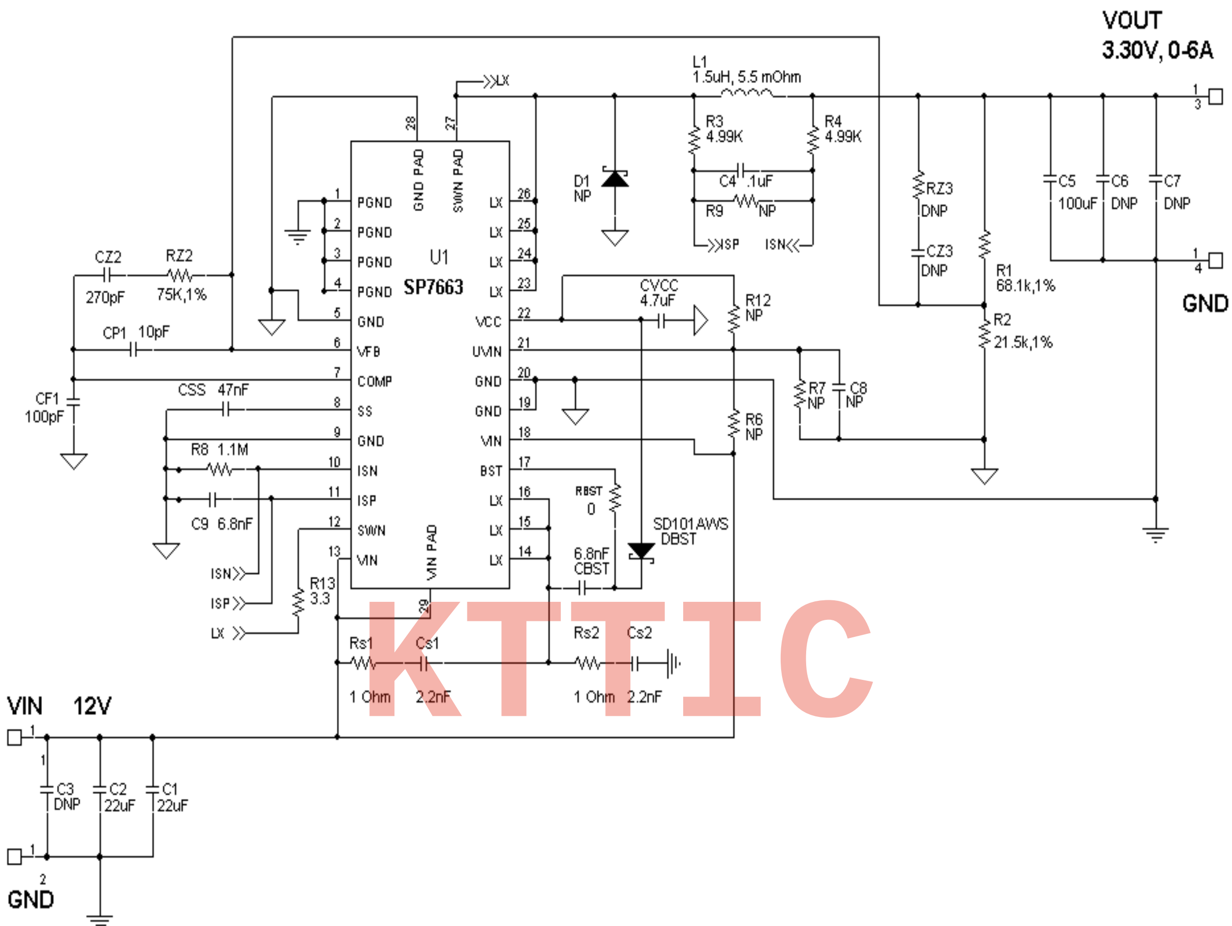
$$CP1 = \frac{1}{\pi \cdot RZ2 \cdot fs}$$

$$CP1 = \frac{1}{\pi \cdot 75K\Omega \cdot 600Khz} = 7.07pF \approx 10pF$$

Cf1 = 100pF to stabilize SP7663ER internal Error Amplifier

OUTPUT WITH A TYPE II COMPENSATION APPLICATION SCHEMATIC

SP76562ER with Tantalum output capacitor configures for VIN = 12V, VOUT = 3.3V at 0-6A output current. Figure 13 and 14 show output voltage ripple to be about 150mV at no load to 6A load. Figure 13 and 14 show a transient response for a load step of 3->6A and 0->6A.



TYPICAL RESULTS FOR TYPE II COMPENSATION

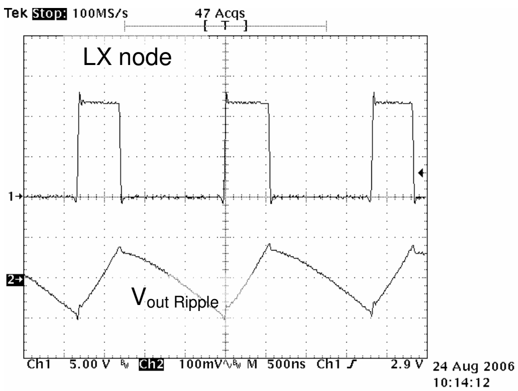


FIGURE 11 VOUT RIPPLE AND LX NODE 6A OUT

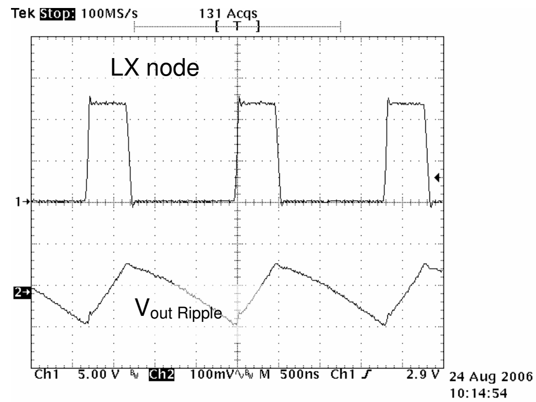


FIGURE 12 VOUT RIPPLE LX NODE 0A OUT

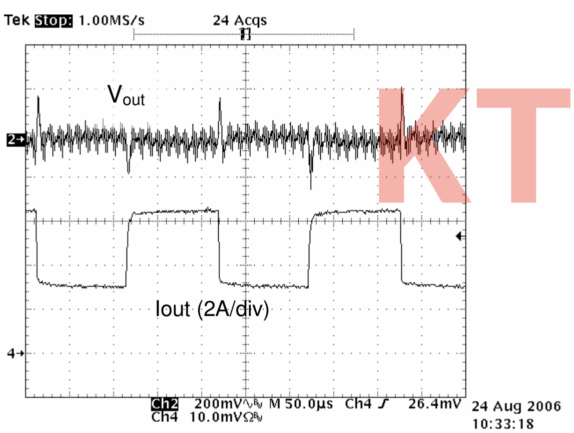


FIGURE 13 TRANSIENT RESPONSE 3->6A

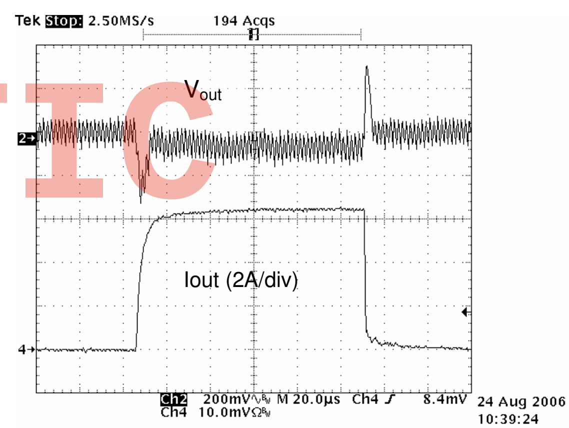


FIGURE 14 VOUT RIPPLE LX NODE 0->6A

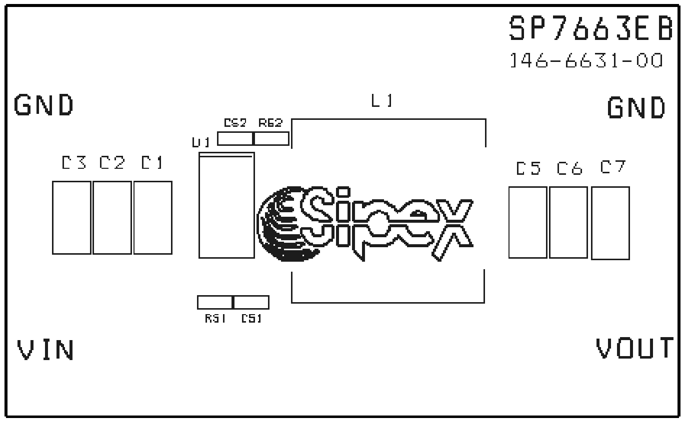


Figure 15. SP7663EB Top Side Component Placement

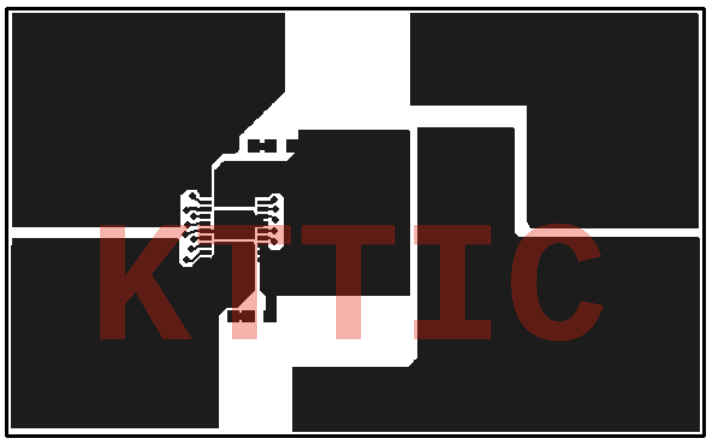


Figure 16. SP7663EB PC Layout Top Side

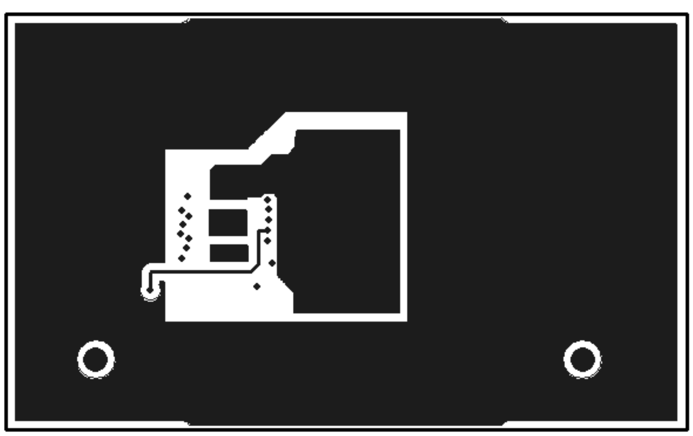


Figure 17. SP7663EB PC Layout 2nd Layer Side

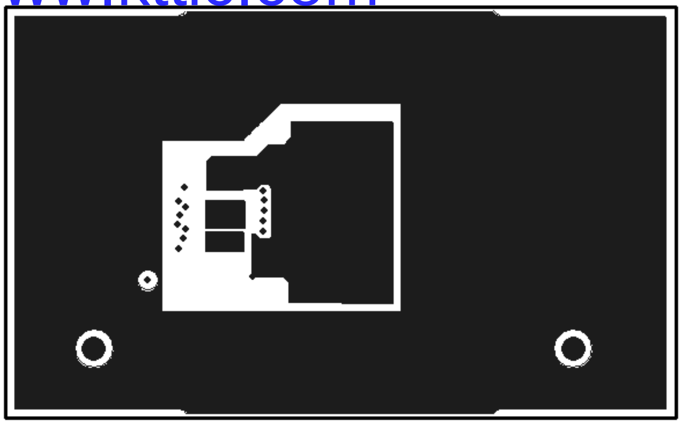


Figure 18. SP7663EB PC Layout 3rd Layer Side

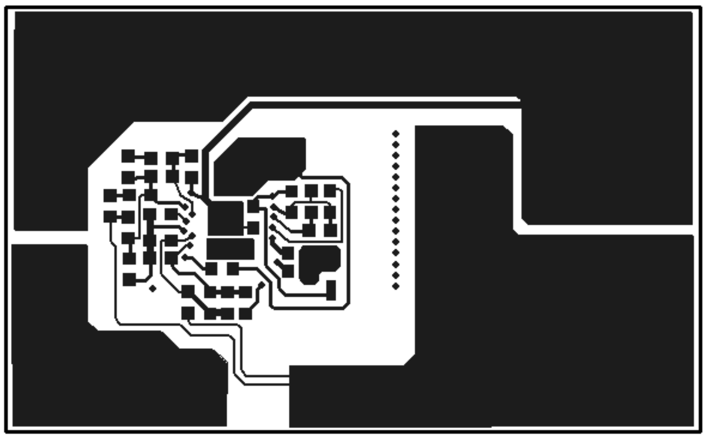


Figure 19. SP7663EB PC Layout Bottom Side

Table 1: SP7663EB Suggested Components and Vendor Lists

Line No.	Ref. Des.	Qty.	Manufacturer	Manuf. Part Number	Layout Size	Component	Vendor Phone #
1	PCB	1	Sipex	146-6631-00		SP7663EB	408-935-7500
2	U1	1	Sipex	SP7663EU	DFN-26	Synchronous Buck Regulator	408-935-7500
3	DBST	1	Vishay Semi	SD101AWS	SOD-323	15mA-30V Schottky Diode	800-344-4539
4	L1	1	Wurth	7443552150	5050	1.5uH Coil, 5.5mΩ	201-785-8800
5	C1, C2,	2	TDK Murata	C3225X5R1C226M GRM32ER61E226K	1210	22uF Ceramic X5R 16V	978-779-3111 770-436-1300
6	C5	1	TDK Murata	C3225X5R0J107M GRM32ER60J107M	1210	100uF Ceramic X5R 6.3V	978-779-3111 770-436-1300
7	C4,	1	TDK	C1608X7R1H104K	0603	0.1uF Ceramic X7R 50V	978-779-3111
8	CBST	1	TDK Murata	C1608X7R1H682K GRM188R71H682KA01	0603	6.8nF Ceramic X7R 50V	978-779-3111 770-436-1300
9	C7, C8, C6, C3	0	Not Populated		0603	Not Populated	
10	C9	1	TDK Murata	C1608X7R1H682K GRM188R71H682KA01	0603	6.8nF Ceramic X7R 50V	978-779-3111 770-436-1300
11	CVCC	1	TDK	C1608X5R1A475M	0603	4.7uF Ceramic X5R 10V	978-779-3111
12	CF1	1	TDK Murata	C1608CH1H101J GRM1885C1H101JA01	0603	100pF Ceramic C0G 50V	978-779-3111 770-436-1300
13	Cs1 Cs2	1	TDK Murata	C1608CH1H222J GRM1885C1H222JA01	0603	2.2nF Ceramic C0G 50V	978-779-3111 770-436-1300
15	CSS	1	TDK Murata	C1608X7R1H473K GRM188R71E473KA01	0603	47nF Ceramic X7R 50V	978-779-3111 770-436-1300
16	CP1	1	TDK	C1608CH1H100J GRM1885C1H100JA01	0603	10pF Ceramic C0G 50V	978-779-3111 770-436-1300
17	CZ3	1	TDK Murata	C1608CH1H181J GRM1885C1H181JA01	0603	180pF Ceramic C0G 50V	978-779-3111 770-436-1300
18	CZ2	1	TDK Murata	C1608CH1H102J GRM1885C1H102JA01	0603	1nF Ceramic C0G 50V	978-779-3111 770-436-1300
19	R1	1	Panasonic	ERJ-3EKF6812V	0603	68.1K Ω Thick Film Res 1%	800-344-4539
20	R2	1	Panasonic	ERJ-3EKF2152V	0603	21.5K Ω Thick Film Res 1%	800-344-4539
21	R3, R4	2	Panasonic	ERJ-3EKF4991V	0603	4.99K Ω Thick Film Res 1%	800-344-4539
22	R12	0	Not Populated		0603	Not Populated	
23	R6, R7	0	Not Populated		0603	Not Populated	
23a	R8	1	Panasonic	ERJ-3EKF1104V	0603	1.1MegΩ Thick Film Res	800-344-4539
24	R9	0	Not Populated		0603	Not Populated	
27	RBST	1	Panasonic	ERJ-3GEYJ00R0V	0603	0 Ω Thick Film Res 1%	800-344-4539
28	Rs1, Rs2	2	Panasonic	ERJ-3GEYJ2R0V	0603	1 Ω Thick Film Res 1%	800-344-4539
29	RZ2	1	Panasonic	ERJ-3EKF2372V	0603	23.2K Ω Thick Film Res 1%	800-344-4539
30	RZ3	1	Panasonic	ERJ-3EKF3091V	0603	3.09K Ω Thick Film Res 1%	800-344-4539
31	VIN, VOUT, GND, GND	4	Vector Electronic	K24C/M	.042 Dia	Test Point Post	800-344-4539

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP7663EB	-40°C to +85°C	SP7663 Evaluation Board
SP7663ER	-40°C to +85°C	26-pin DFN

