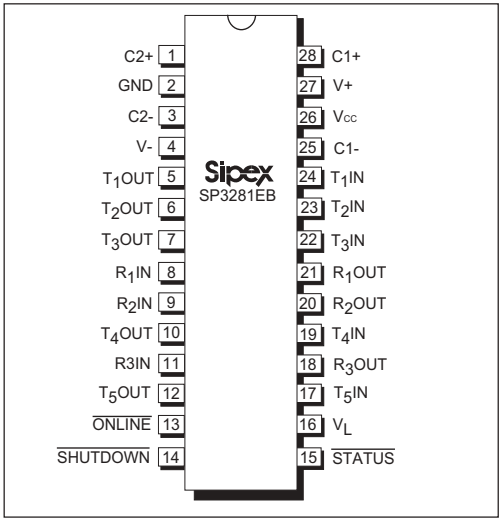
SP3281EB

Intelligent +2.35V to +5.5V RS-232 Transceivers

- Operates over entire Li+ Battery range
- Interoperable with EIA/TIA-232-F and adheres to EIA/TIA-562 down to a +2.35V power supply
- **AUTO ON-LINE®** circuitry automatically wakes up from a 1µA shutdown
- Minimum 250Kbps data rate
- Regulated charge pump yields stable RS-232 outputs regardless of V_{CC} variations
- Unique V_L for low logic compatibility regardless of V_{CC}
- Enhanced ESD Specifications:
  ±15kV Human Body Model
  ±15kV IEC1000-4-2 Air Discharge
  ±8kV IEC1000-4-2 Contact Discharge
- Enhanced battery life as the V_{CC} drops below 3.1V



APPLICATIONS

- Cell phone data cables
- PDAs, PDA cradles
- Hand held equipment
- Peripherals

DESCRIPTION

The SP3281EB device is an RS-232 transceiver solution intended for portable or hand-held applications such as notebook and palmtop computers, PDAs, cell phones and their data cables and cradles.

The SP3281EB is compatible with low voltage logic down to 1.8V using a logic select pin (VL) which conditions the logic inputs and outputs to be compatible with system logic.

The SP3281EB uses an internal high-efficiency, charge-pump power supply that requires only 0.1µF capacitors in 3.3V operation. This charge pump and Sipex's driver architecture allow the SP3281EB device to deliver compliant RS-232 performance from a single +3.3V to +5.5Vpower supply and additionally adhere to EIA/TIA-562 driver outputs levels down to a power supply voltage of 2.35V.

The **AUTO ON-LINE®** feature allows the device to automatically "wake-up" during a shutdown state when an RS-232 cable is connected and a connected peripheral is turned on. Otherwise, the device automatically shuts itself down drawing less than 1µA.

TABLE 1

Device	Power Supplies	RS-232 Drivers	RS232 Receivers	External Components	AUTO ON-LINE® Circuitry	Data Rate	No. of Pins
SP3281EB	2.35V to 5.5V	5	3	4	yes	250kbps	28

Applicable U.S. Patents - 5,306,954; and 6,378,026.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to +6.0V
V+ (note 1).....-0.3V to +7.0V
V- (note 1).....+0.3V to -7.0V
V+ + |V-| (note 1).....+13V
I_{CC} (DC V_{CC} or GND current).....±100mA

Input Voltages

V_L.....-0.3V to +6.0V
TxIN, $\overline{ONLINE}$, $\overline{SHUTDOWN}$, ...0.3V to +6.0V
RxIN.....±25V

Output Voltages

TxOUT.....±13.2V
RxOUT, $\overline{STATUS}$.....-0.3V to (V_L + 0.3V)

Short-Circuit Duration

TxOUT.....Continuous

Storage Temperature.....-65°C to +150°C

Power Dissipation per package

28-pin SSOP
(derate 11.2mW/°C above +70°C).....900mW
28-pin TSSOP
(derate 13.2mW/°C above +70°C).....1100mW

ELECTRICAL CHARACTERISTICS

V_{CC} = +2.35 to +5.5V, V_L=+1.8 to +5.5V, C1 - C4 = 0.22µF.
T_A=T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC}=V_L=+3.3V, and T_A = +25°C.)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SUPPLY CURRENT					
Supply Current, AUTO ON-LINE®		1.0	10	µA	All RxIN open, all TxIN at $V_L$or GND, V_{CC}=V_L=+3.3V, T_A=25°C $\overline{ONLINE}$ = GND, $\overline{SHUTDOWN}$ = V_L,
Supply Current, Shutdown		1.0	10	µA	All RxIN open, all TxIN at V_L or GND V_{CC}=V_L=+3.3V, T_A=25°C $\overline{ONLINE}$ = V_L or GND, $\overline{SHUTDOWN}$ = GND
Supply Current, AUTO ON-LINE® Disabled		0.3	1.0	mA	All TxIN at V_L or GND, $\overline{ONLINE}$ = V_L, V_{CC}=V_L=+3.3V, T_A=25°C $\overline{SHUTDOWN}$ = V_L,no load
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW			0.8 0.6 0.4	V	TxIN, $\overline{ONLINE}$, $\overline{SHUTDOWN}$ V_L = +3.3V or +5.0V V_L = +2.5V V_L = +1.8V
Input Logic Threshold HIGH	2.4 2.0 1.4	0.9		V	TxIN, $\overline{ONLINE}$, $\overline{SHUTDOWN}$ V_L = +5.0V V_L = +3.3V V_L = +2.5V V_L = +1.8V
Transmitter Input Hysteresis		0.3		V	
Input Leakage Current		±0.01	±1.0	µA	TxIN, $\overline{ONLINE}$, $\overline{SHUTDOWN}$, T_A = 25°C
Output Leakage Current		±0.05	±10	µA	RxOUT, Receivers disabled
Output Voltage LOW			0.4 0.4	V	I_{OUT} = +1.6mA, V_L=2.5V, 3.3V, or 5.0V I_{OUT} = +0.8mA, V_L=1.8V
Output Voltage HIGH	V_L - 0.6 V_L - 0.6	V_L - 0.1 V_L - 0.1		V	I_{OUT} = -1.0mA, V_L=2.5V, 3.3V, 5.0V I_{OUT} = -0.5mA, V_L=1.8V
DRIVER OUTPUTS					
V_{CC} Mode Switch Point (V_{CC} is Falling)	2.95	3.1	3.25	V	TxOUT=±5.0V to ±3.7V
V_{CC} Mode Switch Point (V_{CC} is Rising)	3.3	3.5	3.7	V	TxOUT=±3.7V to ±5.0V
V_{CC} Mode Switch Point Hysteresis		400		mV	

ELECTRICAL CHARACTERISTICS: Continued

V_{CC} = +2.35 to +5.5V, V_L=+1.8 to +5.5V, C1 - C4 = 0.22µF.
T_A=T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC}=V_L=+3.3V, and T_A = +25°C.)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Output Voltage Swing	±5.0 +/-3.7	±5.4		V	All driver outputs loaded with 3KΩ to GND, T_A=25°C V_{CC}=3.25V to 5.5V, V_{CC}=2.35 to 2.95V,
Output Resistance	300			Ω	V_{CC} = V+ = V- = 0V, V_{TXOUT} = ±2V
Output Short-Circuit Current		±35	±60	mA	V_{TXOUT} = GND
Ouput Leakage Current			+/-25	µA	V_{TXOUT}=+/-12V, transmitter disabled, V_{CC}=0V or 2.35V to 5.5V
RECEIVER INPUTS					
Input Voltage Range	-25		25	V	
Input Threshold LOW	0.3 0.6 0.8	0.8 1.2 1.5		V	VL=1.8V, T_A=25°C VL=2.5V or 3.3V, T_A=25°C VL=5.0V, T_A=25°C
HIGH		1.0 1.5 1.8	1.8 2.4 2.4	V	VL=1.8V, T_A=25°C VL=2.5V or 3.3V, T_A=25°C VL=5.0V, T_A=25°C
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	kΩ	T_A=25°C
AUTO ON-LINE® CIRCUITRY CHARACTERISTICS ($\overline{ONLINE}$ = GND, $\overline{SHUTDOWN}$ = V_{CC})					
$\overline{STATUS}$ Output Voltage					
LOW			0.4	V	I_{OUT} = 1.6mA, V_L=2.5V, 3.3V, 5.0V or I_{OUT} = +0.8mA, V_L=1.8V
HIGH	V_L - 0.6	V_L-0.1			I_{OUT} = -1.0mA, V_L=2.5V, 3.3V, 5.0V or I_{OUT} = -0.5mA, V_L=1.8V
Receiver Threshold to Drivers Enabled (t_{ONLINE})		200		µs	
Receiver +/- Threshold to $\overline{Status}$ HIGH (t_{STSH}) to $\overline{Status}$ LOW (t_{STSL})		20 20		µs µs	
AC Characteristics					
Maximum Data Rate	250			kbps	SP3281EB: R_L = 3kΩ, C_L = 1000pF, one driver switching
Receiver Propagation Delay t_{PHL} t_{PLH}		0.15 0.15		µs	Receiver input to output, C_L = 150pF
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Time to Exit Shutdown		100		µs	$\|V_{TXOUT}\|$>3.7V, V_{CC}=3.3V
Driver Skew $\|t_{PHL}-tP_{LH}\|$		100		ns	Measured at zero crossover
Receiver Skew $\|t_{PHL}-t_{PLH}\|$		50		ns	Measured at zero crossover
Transition-Region Slew Rate			30	V/µs	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ , T_A = 25°C, measurements taken from -3.0V to+3.0V or +3.0V to -3.0V C_L = 150pF to 1000pF

PIN DESCRIPTION

NAME	FUNCTION	PIN NO.
C2+	Positive terminal of the symmetrical charge-pump capacitor C2.	1
GND	Ground.	2
C2-	Negative terminal of the symmetrical charge-pump capacitor C2.	3
V-	Regulated -4.0V or -5.5V output generated by the charge pump.	4
T_1OUT	RS-232 driver output.	5
T_2OUT	RS-232 driver output.	6
T_3OUT	RS-232 driver output.	7
R_1IN	RS-232 receiver input.	8
R_2IN	RS-232 receiver input.	9
T_4OUT	RS-232 driver output.	10
R_3IN	RS-232 receiver input.	11
T_5OUT	RS-232 driver output.	12
$\overline{\text{ONLINE}}$	Apply logic HIGH to override AUTO ON-LINE® circuitry keeping drivers active ($\overline{\text{SHUTDOWN}}$ must also be logic HIGH, refer to Table 2).	13
$\overline{\text{SHUTDOWN}}$	Apply logic LOW to shut down drivers and charge pump. This overrides all AUTO ON-LINE® circuitry and $\overline{\text{ONLINE}}$ (refer to Table 2).	14
$\overline{\text{STATUS}}$	TTL/CMOS Output indicating if a RS-232 signal is present on any Rx input.	15
V_L	Logic level supply voltage selection	16
T_5IN	TTL/CMOS driver input.	17
R_3OUT	TTL/CMOS receiver output.	18
T_4IN	TTL/CMOS driver input.	19
R_2OUT	TTL/CMOS receiver output.	20
R_1OUT	TTL/CMOS receiver output.	21
T_3IN	TTL/CMOS driver input.	22
T_2IN	TTL/CMOS driver input.	23
T_1IN	TTL/CMOS driver input.	24
C1-	Negative terminal of the symmetrical charge-pump capacitor C1.	25
V_{CC}	+2.35V to +5.5V supply voltage.	26
V+	Regulated +4.0V or +5.5V output generated by the charge pump.	27
C1+	Positive terminal of the symmetrical charge-pump capacitor C1	28

Table 2. Device Pin Description

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +4.2V, 250kbps data rate, all drivers loaded with 3kΩ, 0.22µF charge pump capacitors, and T_{AMB} = +25°C.

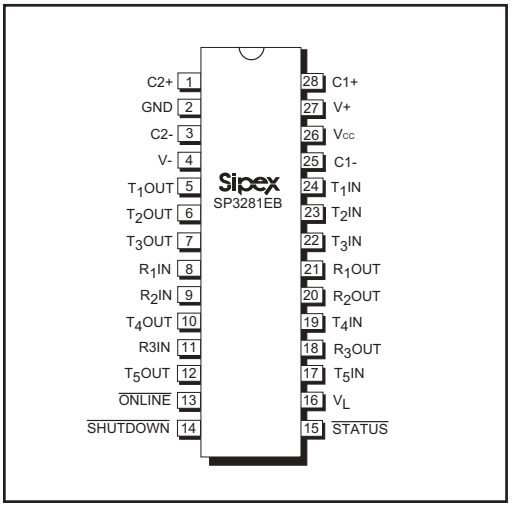


Figure 2. SP3281EB Pinout Configuration

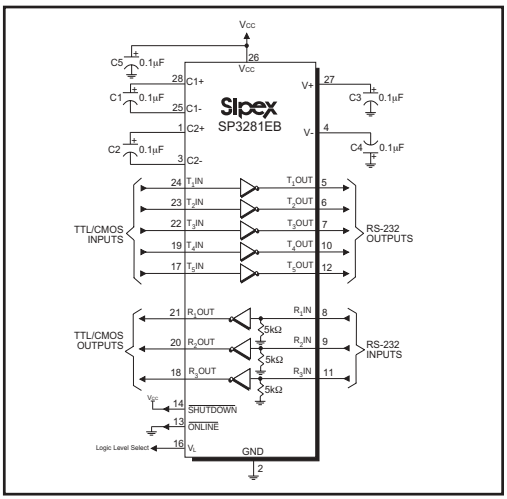


Figure 3. SP3281EB Application Diagram

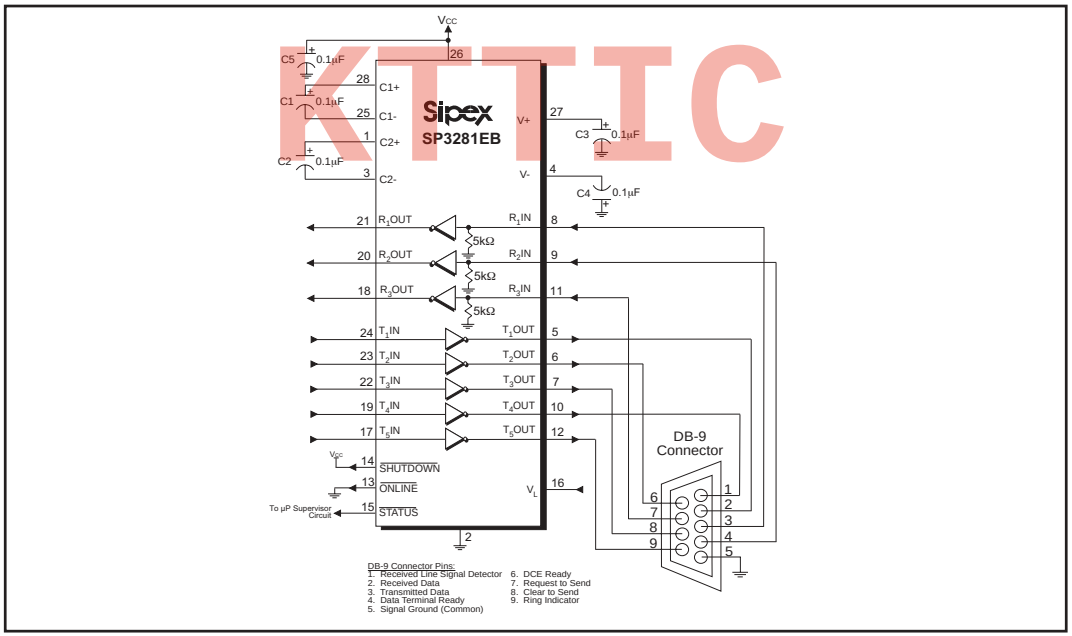


Figure 4. Circuit for the connectivity of the SP3281EB with a DB-9 connector

DESCRIPTION

The SP3281EB device meets the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The SP3281EB device features Sipex's proprietary and patented (U.S. #5,306,954) on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.3V to +5.5V power supply. The SP3281EB will adhere to EIA/TIA-562 voltage levels with V_{CC} as low as 2.35V.

The SP3281EB device is an ideal choice for power sensitive designs. The SP3281EB device features AUTO ON-LINE® circuitry which reduces the power supply drain to a 1µA supply current. In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

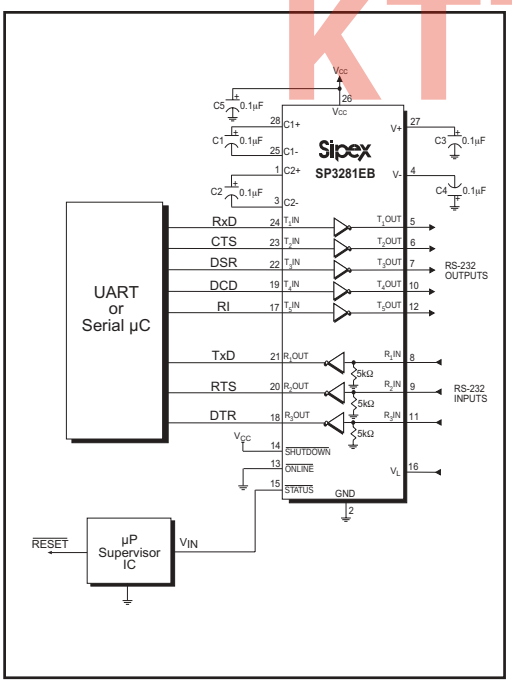


Figure 5. Interface Circuitry Being Controlled by Microprocessor Supervisory Circuit

THEORY OF OPERATION

The SP3281EB device is made up of four basic circuit blocks: 1. Drivers, 2. Receivers, 3. The Sipex proprietary charge pump, and 4. AUTO ON-LINE® circuitry.

Drivers

The drivers are inverting level transmitters that , when V_{CC} is between +3.3V and +5.5V, convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels . Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232F and all previous RS-232 versions. The driver outputs will adhere to EIA/TIA-562 when V_{CC} is as low as 2.35V.

The SP3281EB drivers can guarantee a data rate of 250 kbps fully loaded with 3kΩ in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software. All unused driver inputs must be connected to V_L or GND.

Figure 6 shows a loopback test circuit used to test the SP3281EB RS-232 drivers. Figure 7 shows the test results of the loopback circuit with all five drivers active at 120kbps with typical RS-232 loads in parallel with 1000pF capacitors. Figure 8 shows the test results where one driver was active at 250kbps and all five drivers loaded with an RS-232 receiver in parallel with a 1000pF capacitor. A solid RS-232 data transmission rate of 120kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

Receivers

The receivers convert ±5.0V EIA/TIA-232 levels to TTL or CMOS logic output levels.

Receivers are not active when in shutdown. If there is no activity present at the receivers for a period longer than 100µs during AUTO ON-LINE® mode or when $\overline{\text{SHUTDOWN}}$ is enabled, the device goes into a standby mode where the circuit draws 1µA. The truth table logic of the driver and receiver outputs can be found in Table 3.

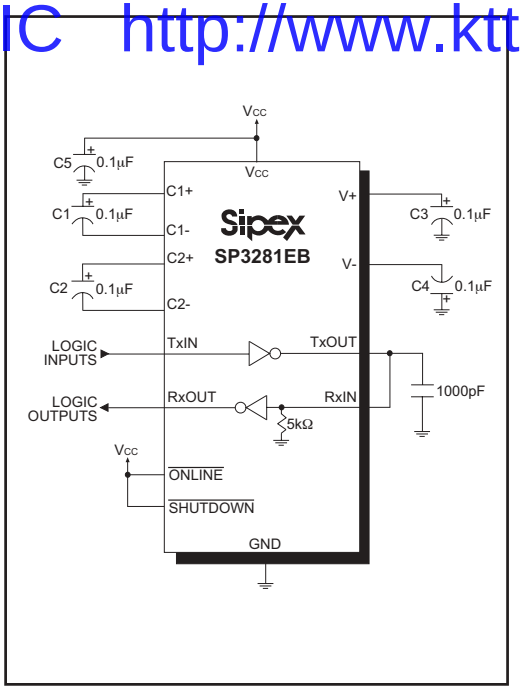


Figure 6. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

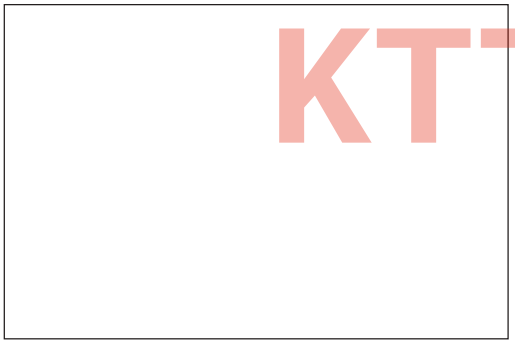


Figure 7. Loopback Test Circuit Result at 120kbps (All Drivers Fully Loaded)

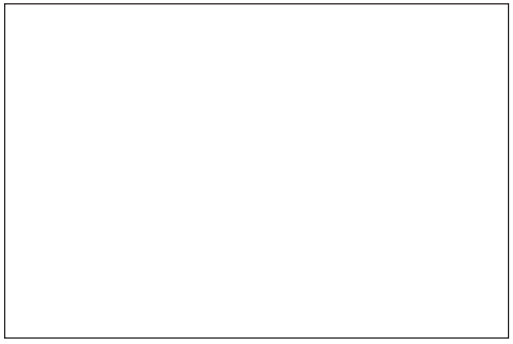


Figure 8. Loopback Test Circuit result at 250kbps (All Drivers Fully Loaded)

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is a Sipex–patented design (U.S. #5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump uses a four–phase voltage shifting technique to attain symmetrical ±5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages ±5.5V regardless of the input voltage (V_{CC}) over the +3.3V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations. The charge pump will provide output voltage levels of ±4.0V when the input voltage (V_{CC}) is from +3.1V to +2.35V.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V (V_{CC} > 3.3V) and 4.0V (V_{CC} < 3.1V), the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V (V_{CC} > 3.3V) and 4.0V (V_{CC} < 3.1V), the charge pump is disabled. This oscillator controls the four phases of the voltage shifting (Figure 10).

A description of each phase follows.

Phase 1 (Figure 11)

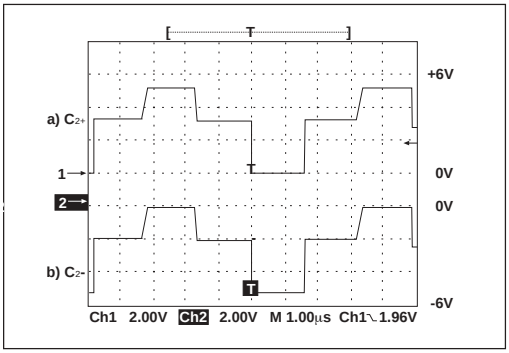


Figure 10. Charge Pump Waveforms

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2 (Figure 12)
— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V (V_{CC} > 3.3V) and -4.0V (V_{CC} < 3.1V).
Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3 (Figure 13)
— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4 (Figure 14)
— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V (V_{CC}>3.3V) and +4.0V(V_{CC}<3.1V). At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for theinternal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC} in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 500kHz. The external capacitors should be 0.22µF with a 16V working voltage rating for a V_{CC} input range of +2.35V to +5.5V.

Charge Pump Capacitor Selection

The charge pump capacitors C1-C4 and bypass C5 can be of any type including ceramic. If polarized capacitors are used, refer to figure 3 application diagram for proper orientation. The following chart illustrates the minimum capacitor valve for a given input voltage range.

V_{CC} (V)	C1 and C5 (µF)	C2,C3,C4 (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
2.35 to 5.5	0.22	0.22

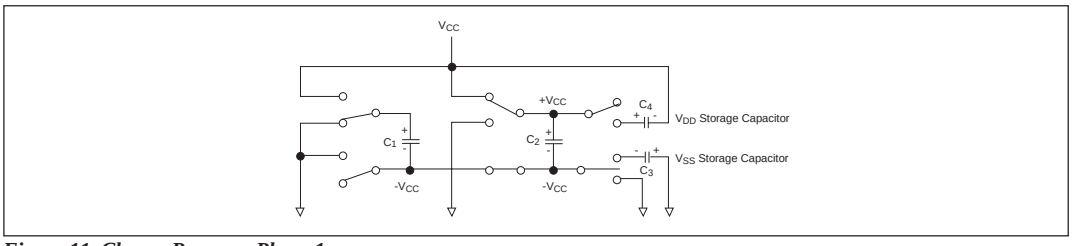


Figure 11. Charge Pump — Phase 1

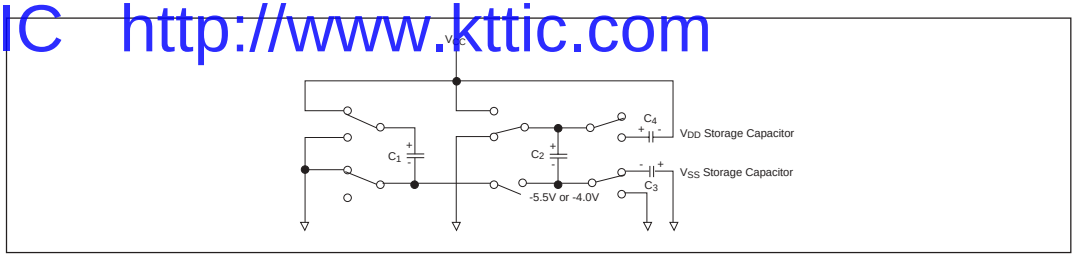


Figure 12. Charge Pump — Phase 2

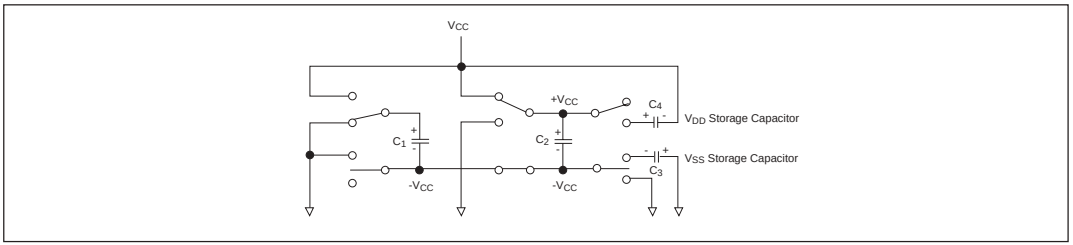


Figure 13. Charge Pump — Phase 3

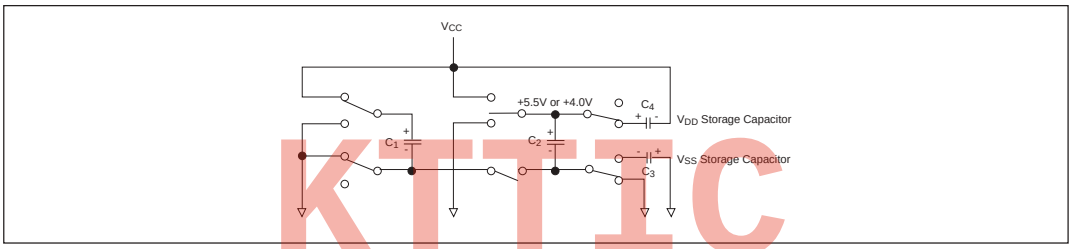


Figure 14. Charge Pump — Phase 4

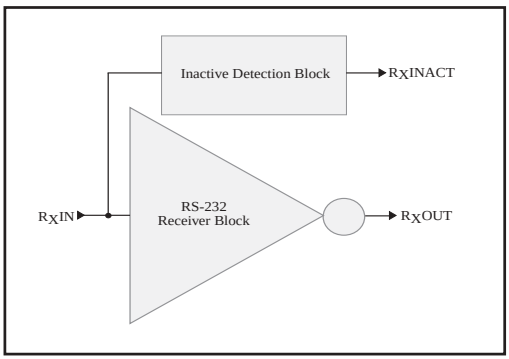


Figure 15. Stage I of AUTO ON-LINE® Circuitry

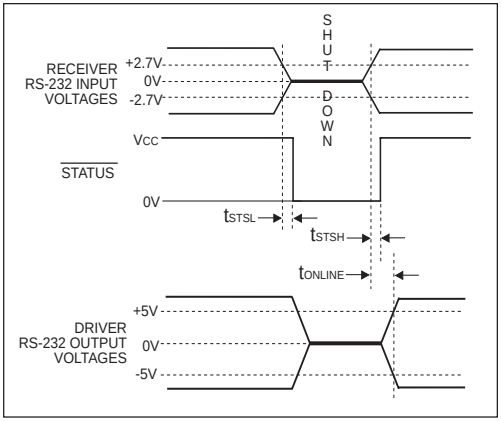


Figure 17. AUTO ON-LINE® Timing Waveforms

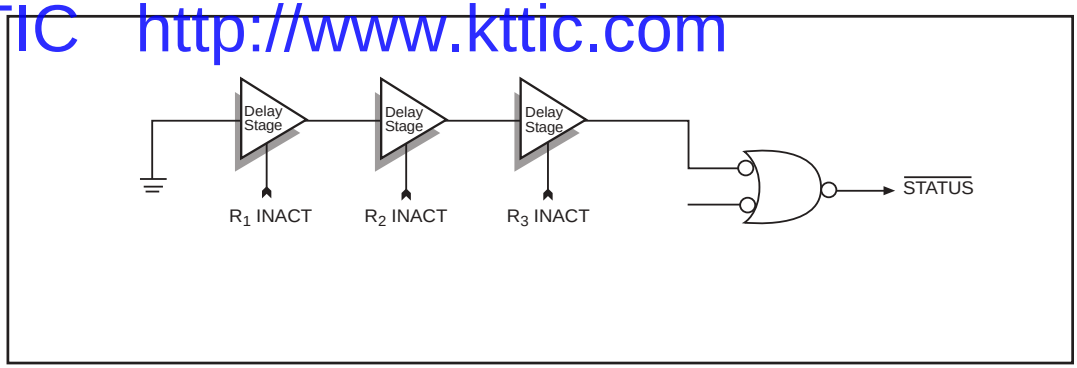


Figure 16. Stage II of AUTO ON-LINE® Circuitry

SHUTDOWN INPUT	ONLINE INPUT	RS-232 SIGNAL AT RECEIVER INPUT	STATUS OUTPUT	T_xOUT	R_xOUT	TRANSCEIVER STATUS
HIGH	-	YES	HIGH	Active	Active	Normal Operation
HIGH	HIGH	NO	LOW	Active	Active	Normal Operation
HIGH	LOW	NO	LOW	High-Z	Active	AUTO ON-LINE® Mode
LOW	-	YES	HIGH	High-Z	High-Z	Shutdown
LOW	-	NO	LOW	High-Z	High-Z	Shutdown

Table 3. AUTO ON-LINE® Logic

AUTO ON-LINE® Circuitry

The SP3281EB device has a patent pending AUTO ON-LINE® circuitry on board that saves power in applications such as laptop computers, palmtop (PDA) computers, and other portable systems.

The SP3281EB device incorporates an AUTO ON-LINE® circuit that automatically enables itself when the external transmitters are enabled and the cable is connected. Conversely, the AUTO ON-LINE® circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1µA. This function is controlled by the $\overline{\text{ONLINE}}$ pin. When this pin is tied to a logic LOW, the AUTO ON-LINE® function is active. Once active, the device is enabled until there is no activity on the receiver inputs. The receiver input typically sees at least ±3V, which are generated from the transmitters at the other end of the cable with a ±5V minimum. When the external transmitters are disabled or the cable is disconnected, the receiver inputs will be pulled down by their internal 5kΩ resistors to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standby mode. When $\overline{\text{ONLINE}}$ is HIGH, the AUTO ON-LINE® mode is disabled.

The AUTO ON-LINE® circuit has two stages:

1) Inactive Detection
2) Accumulated Delay

The first stage, shown in Figure 15, detects an inactive input. A logic HIGH is asserted on R_XINACT if the cable is disconnected or the

external transmitters are disabled. Otherwise, R_XINACT will be at a logic LOW. This circuit is duplicated for each of the other receivers.

The second stage of the AUTO ON-LINE® circuitry, shown in Figure 16, processes all the receiver's R_XINACT signals with an accumulated delay that disables the device to a 1µA supply current. The $\overline{STATUS}$ pin goes to a logic LOW when the cable is disconnected, or when the external transmitters are disabled.

When the drivers or internal charge pump are disabled, the supply current is reduced to 1µA. This can commonly occur in hand-held or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are turned off.

The AUTO ON-LINE® mode can be disabled by the $\overline{SHUTDOWN}$ pin. If this pin is a logic LOW, the AUTO ON-LINE® function will not operate regardless of the logic state of the $\overline{ONLINE}$ pin. Table 3 summarizes the logic of the AUTO ON-LINE® operating modes and the truth table logic of the driver and receiver outputs.

When the SP3281EB device is shut down, the charge pump is turned off. V+ charge pump output decays to V_{CC}, the V- output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V+ and V- levels is typically 200µs.

For easy programming, the $\overline{STATUS}$ pin can be used to indicate DTR or a Ring Indicator signal. Tying $\overline{ONLINE}$ and $\overline{SHUTDOWN}$ together will bypass the AUTO ON-LINE® circuitry so this connection acts like a shutdown input pin.

ESD TOLERANCE

The SP3281EB device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC1000-4-2 Air-Discharge
c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 18. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on Figure 19. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was

devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit model in Figures 18 and 19 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

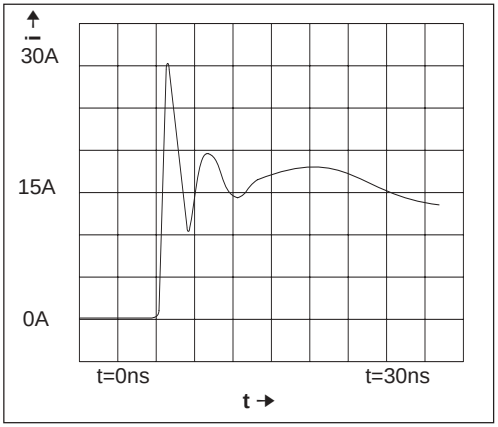


Figure 20. ESD Test Waveform for IEC1000-4-2

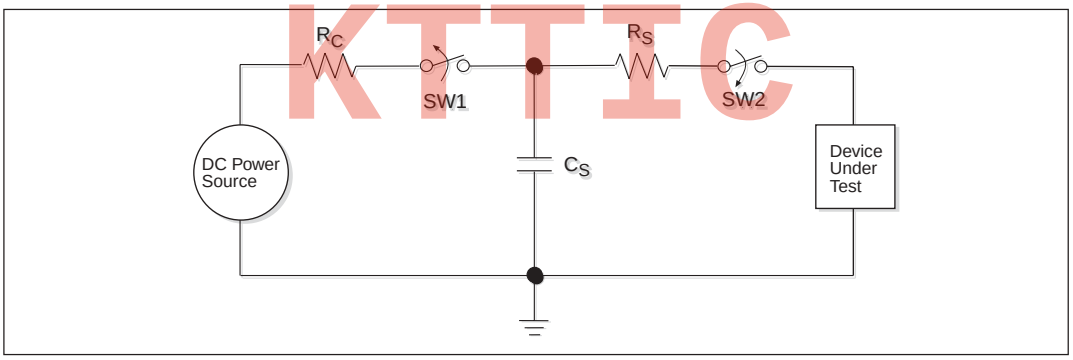


Figure 18. ESD Test Circuit for Human Body Model

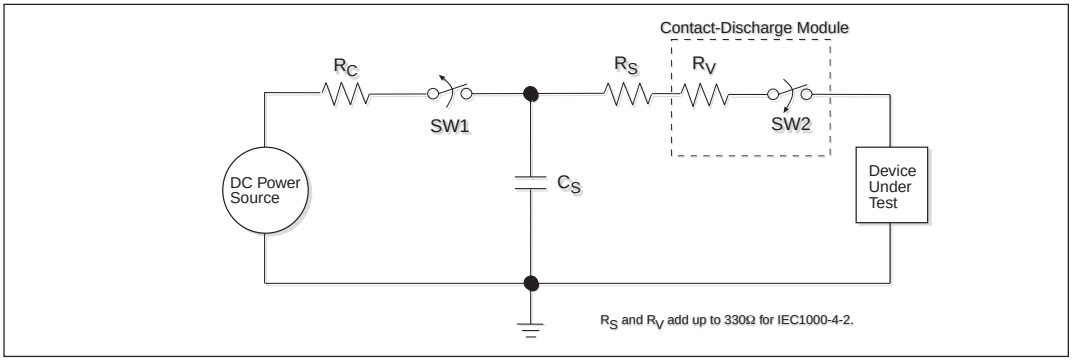
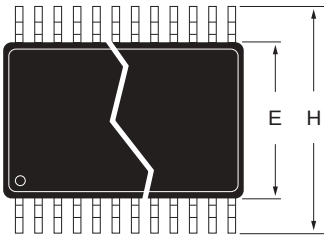


Figure 19. ESD Test Circuit for IEC1000-4-2

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs Receiver Inputs	±15kV ±15kV	±15kV ±15kV	±8kV ±8kV	4 4

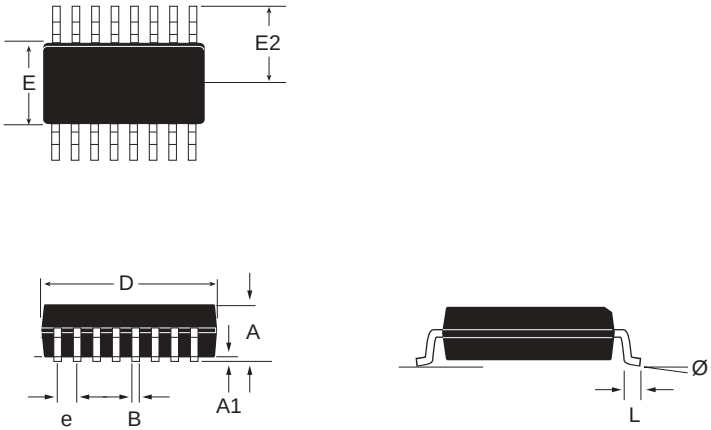
Table 4. Transceiver ESD Tolerance Levels

PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)



DIMENSIONS (Inches) Minimum/Maximum (mm)	28–PIN
A	0.068/0.078 (1.73/1.99)
A1	0.002/0.008 (0.05/0.21)
B	0.010/0.015 (0.25/0.38)
D	0.397/0.407 (10.07/10.33)
E	0.205/0.212 (5.20/5.38)
e	0.0256 BSC (0.65 BSC)
H	0.301/0.311 (7.65/7.90)
L	0.022/0.037 (0.55/0.95)
Ø	0°/8° (0°/8°)

PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)



DIMENSIONS in inches (mm) Minimum/Maximum	28–PIN
A	- /0.043 (- /1.10)
A1	0.002/0.006 (0.05/0.15)
B	0.007/0.012 (0.19/0.30)
D	0.378/0.386 (9.60/9.80)
E	0.169/0.177 (4.30/4.50)
e	0.026 BSC (0.65 BSC)
E2	0.126BSC (3.20BSC)
L	0.020/0.030 (0.50/0.75)
Ø	0°/8°

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP3281EBCA	0°C to +70°C	28-pin SSOP
SP3281EBCY	0°C to +70°C	28-pin TSSOP
SP3281EBEA	40°C to +85°C	28-pin SSOP
SP3281EBEY	40°C to +85°C	28-pin TSSOP

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Sipex Corporation

ANALOG EXCELLENCE

Sipex Corporation

Headquarters and Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600

Sales Office
22 Linnell Circle
Billerica, MA 01821
TEL: (978) 667-8700
FAX: (978) 670-9001
e-mail: sales@sipex.com

