



# Low Noise Dual 300mA LDO with Independent Shutdown

## DESCRIPTION

The EUP7559 is a dual low dropout linear regulator capable of sourcing 300mA current per regulator.

The EUP7559 is stable with small ceramic output capacitors. The performance of EUP7559 is optimized for battery power systems to deliver low noise, low dropout voltage, low quiescent current and excellent line and load transient response.

The EUP7559 is available in fixed output voltages in the 8-pin 3mmx3mm TDFN leadless package.

## FEATURES

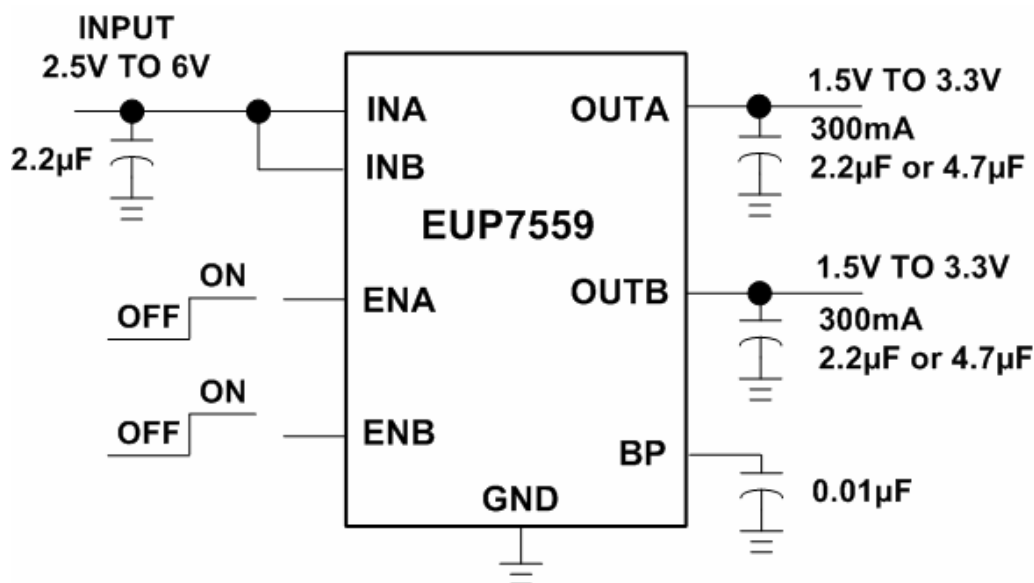
- Input Voltage Range: 2.5V to 6V
- 300mA Output Current per LDO
- Low Dropout Voltage of 55mV@100mA
- Low Quiescent Current of 115µA per LDO
- High PSRR 70dB at 1kHz
- Low Output Noise
- Thermal Shutdown Protection
- Current Limit Protection
- Separate Enable pin per LDO
- Stable with Ceramic Output Capacitor
- 1.5V to 3.3V Pre-set Output
- 3mmx3mm TDFN-8 Package
- RoHS Compliant and 100% Lead (Pb)-Free

## APPLICATIONS

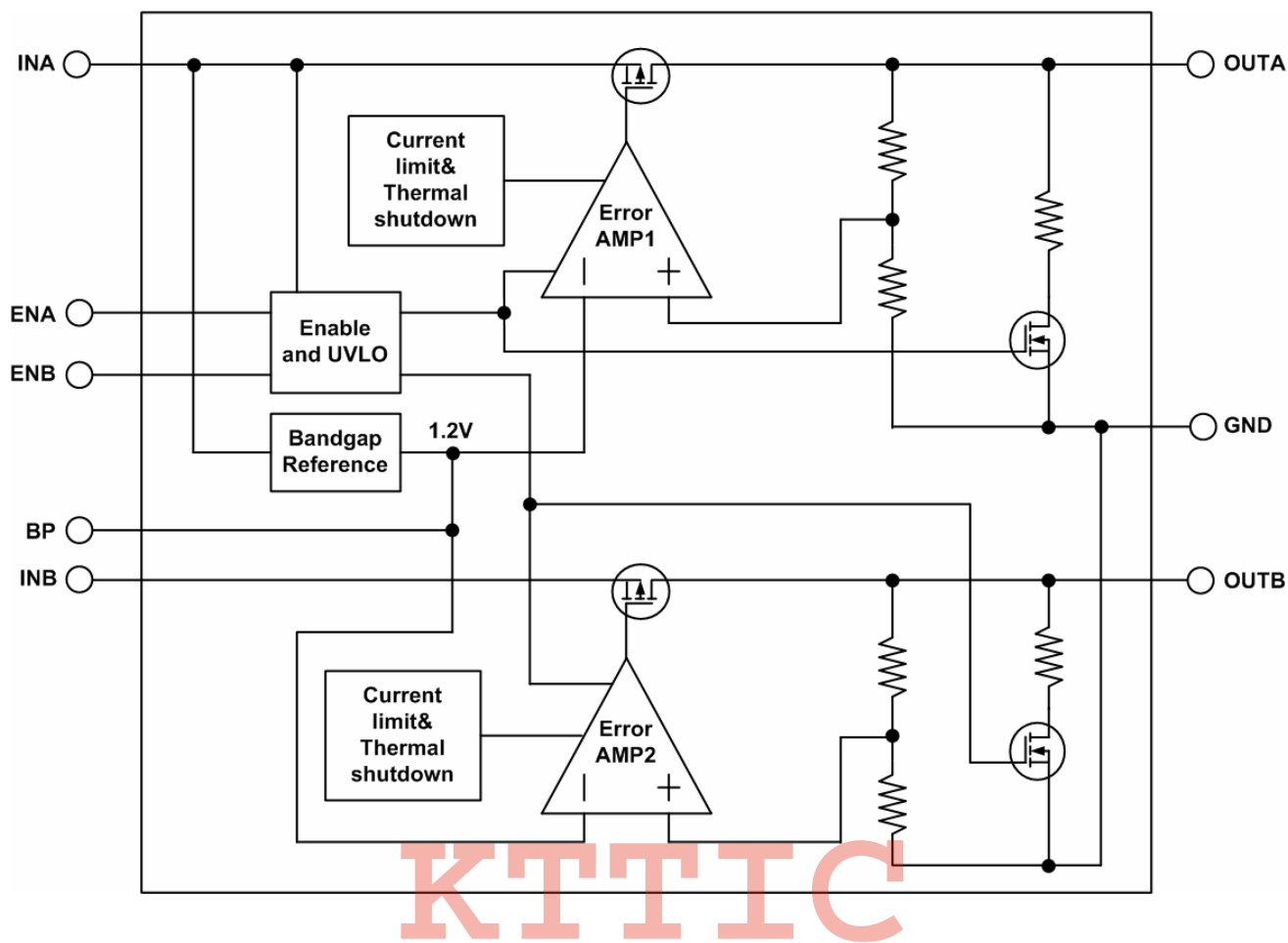
- Cellular Phones
- PDAs and Palmtop Computers
- Wireless LAN Cards
- Hand-Held Instruments



## Typical Application



Block Diagram



**Pin Configurations**

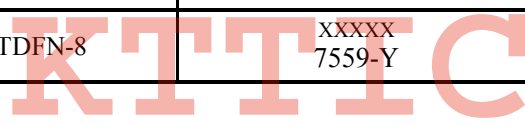
Package Type	Pin Configurations
TDFN-8	<p style="text-align: center;">TOP VIEW</p> <p style="text-align: center;">             INA 1 8 OUTA              ENA 2 7 BP              ENB 3 6 GND              INB 4 5 OUTB         </p>

**Pin Description**

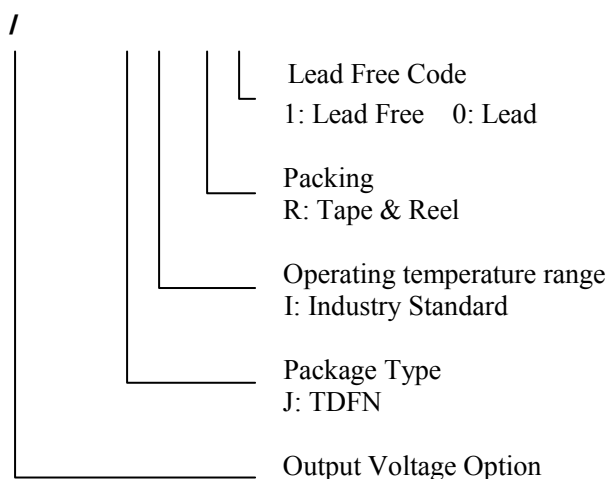
PIN	Pin	DESCRIPTION
INA	1	LDO A Regulator Input. Connect to INB. Input voltage can range from 2.5V to 6V. Bypass INA with a ceramic capacitor to GND.
ENA	2	Shutdown A Input. A logic-low on ENA shuts down regulator A. If ENA and ENB are both low, both regulators and the internal reference are off and the supply current is reduced to 10nA (typ). If either ENA or ENB is a logic high, the internal reference is on. Connect ENA to INA for always-on operation of regulator A.
ENB	3	Shutdown B Input. A logic-low on ENB shuts down regulator B. If ENA and ENB are both low, both regulators and the internal reference are off and the supply current is reduced to 10nA (typ). If either ENA or ENB is a logic high, the internal reference is on. Connect ENB to INB for always-on operation of regulator B.
INB	4	LDO B Regulator Input. Connect to INA. Input voltage can range from 2.5V to 6V. Bypass INB with a ceramic capacitor to GND.
OUTB	5	Regulator B Output. OUTB can source up to 300mA continuous current. Bypass OUTB with a ceramic capacitor to GND. During shutdown, OUTB is internally discharged to GND through a 300 Ω resistor.
GND	6	Ground.
BP	7	Reference Noise Bypass. Bypass BP with a low-leakage 0.01μF ceramic capacitor for reduced noise at both outputs.
OUTA	8	Regulator A Output. OUTA can source up to 300mA continuous current. Bypass OUTA with a ceramic capacitor to GND. During shutdown, OUTA is internally discharged to GND through a 300 Ω resistor.

**Ordering Information**

Order Number	Package Type	Marking	Operating Temperature range
EUP7559-1.5/1.5JIR1	TDFN-8	XXXXX 7559-V	-40 °C to 125°C
EUP7559-1.5/2.8JIR1	TDFN-8	XXXXX 7559-C	-40 °C to 125°C
EUP7559-1.8/2.8JIR1	TDFN-8	XXXXX 7559-A	-40 °C to 125°C
EUP7559-1.8/3.3JIR1	TDFN-8	XXXXX 7559-H	-40 °C to 125°C
EUP7559-1.85/1.5JIR1	TDFN-8	XXXXX 7559-a	-40 °C to 125°C
EUP7559-2.5/2.8JIR1	TDFN-8	XXXXX 7559-D	-40 °C to 125°C
EUP7559-2.85/1.8JIR1	TDFN-8	XXXXX 7559-b	-40 °C to 125°C
EUP7559-2.85/1.85JIR1	TDFN-8	XXXXX 7559-X	-40 °C to 125°C
EUP7559-2.85/2.85JIR1	TDFN-8	XXXXX 7559-G	-40 °C to 125°C
EUP7559-3.15/2.8JIR1	TDFN-8	XXXXX 7559-Z	-40 °C to 125°C
EUP7559-3.3/2.85JIR1	TDFN-8	XXXXX 7559-W	-40 °C to 125°C
EUP7559-3.3/3.0JIR1	TDFN-8	XXXXX 7559-Y	-40 °C to 125°C



EUP7559



**Absolute Maximum Ratings**

- $V_{IN}, V_{EN}$  ----- -0.3V to 6.5V
- Power Dissipation ( $P_D$ ) ----- Internally Limited
- Junction Temperature ----- -40°C to +125°C
- Storage Temperature ----- -65°C to +150°C
- Lead Temp ----- 260°C

**Operating Ratings**

- $V_{IN}$  ----- 2.5 to 6V
- $V_{EN}$  ----- 0V to 6V
- Junction Temperature ----- 150°C
- Thermal Resistance  $\theta_{JA}$ (TDFN-8) ----- 60°C/W

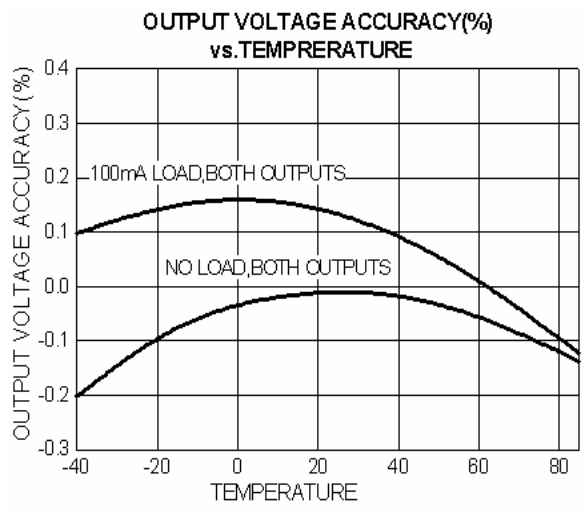
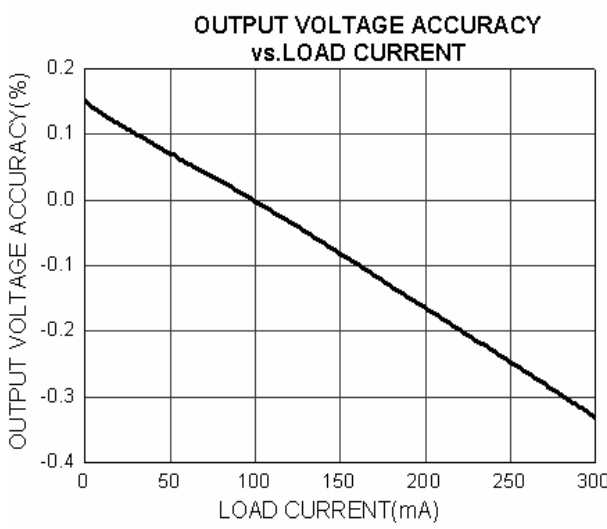
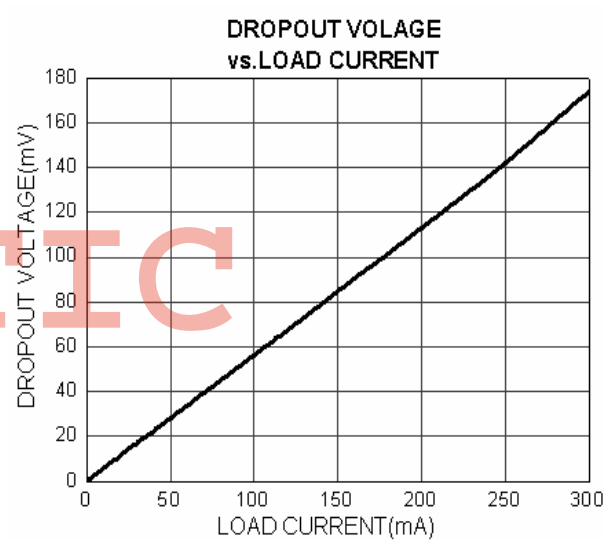
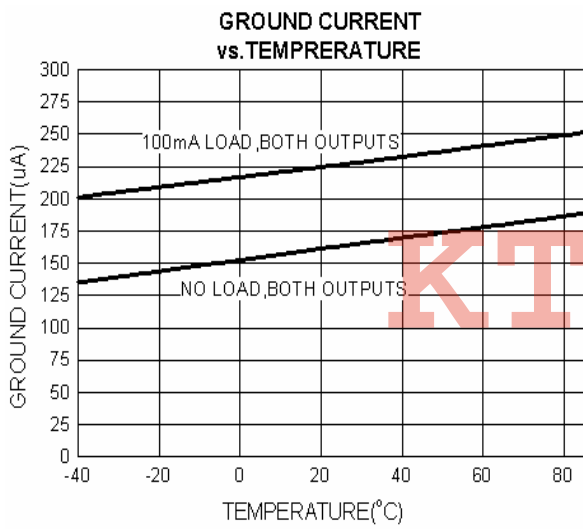
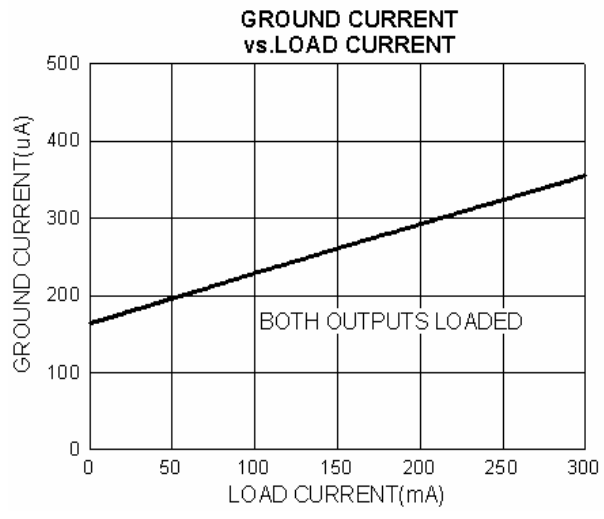
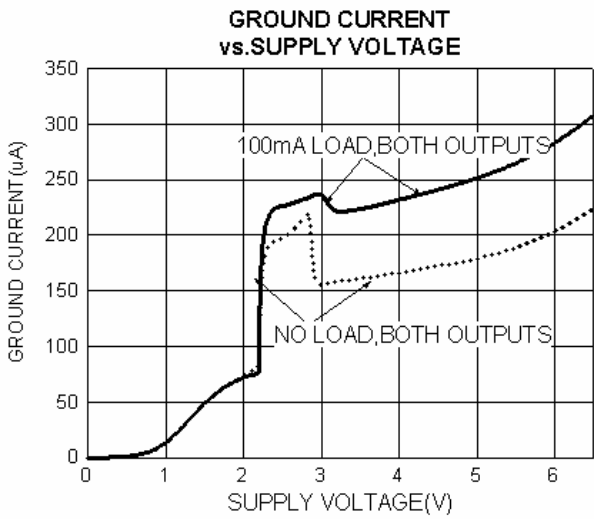
**Electrical Characteristics**

$V_{IN}=3.8V, V_{ENA}=V_{ENB}=V_{IN}, I_o=10mA, C_{IN}=C_{OUT}=2.2\mu F, T_A = -40^\circ C \sim 85^\circ C.$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	$V_{IN}$		2.5		6	V
Undervoltage-Lockout Threshold	$V_{UVLO}$	$V_{IN}$ Rising , hysteresis is 40mV(typ)	2.15	2.3	2.45	V
Output Voltage Accuracy	$V_o$	$T_A=25^\circ C, I_{OUT1}=I_{OUT2}=1mA$	-1.5		1.5	%
		$T_A=-40^\circ C$ to $85^\circ C, I_{OUT1}=I_{OUT2}=1mA$	-2.5		2.5	
		$T_A=-40^\circ C$ to $85^\circ C, I_{OUT1}$ or $I_{OUT2}=0.1mA$ to 300mA	-3		3	
Maximum Output Current	$I_{OUT}$		300			mA
Output Current Limit	$I_{LIM}$		320	500	780	mA
Ground Current	$I_Q$	No Load		180	280	$\mu A$
		No Load, one LDO Shutdown		115		
		$I_{OUT1}=I_{OUT2}=100mA$		240		
Dropout Voltage	$V_{IN}-V_{OUT}$	$I_{OUT}=1mA$		0.6		mV
		$I_{OUT}=100mA$		55	110	
Line Regulation	$V_{LNR}$	$V_{IN}=(V_o+0.1)V$ to 6V, $I_{OUT}=1mA$	-0.15	0.02	0.15	%V
Output Voltage Noise		100Hz to 100kHz, $C_{OUT}=10\mu F, I_{OUT}=1mA, C_{BP}=0.01\mu F$		35		$\mu V_{rms}$
		100Hz to 100kHz, $C_{OUT}=10\mu F, I_{OUT}=1mA, C_{BP}$ =not installed		124		
Power Supply Ripple Rejection	PSRR	$C_{OUT}=2.2\mu F, I_{OUT}=50mA, C_{BP}=0.01\mu F, f=1kHz$		70		dB
		$C_{OUT}=2.2\mu F, I_{OUT}=50mA, C_{BP}=0.01\mu F, f=10kHz$		60		
		$C_{OUT}=2.2\mu F, I_{OUT}=50mA, C_{BP}=0.01\mu F, f=100kHz$		46		
Shutdown Supply Current	$I_{SHDN}$	$V_{EN}=0, T_A=25^\circ C$		0.01	1	$\mu A$
		$T_A=-40^\circ C$ to $85^\circ C$		0.1		
Enable Input Threshold	$V_{IH}$	Input high voltage	1.6			V
	$V_{IL}$	Input low voltage			0.4	
Enable Input Bias Current		$V_{EN}=0$ or IN, $T_A=25^\circ C$		0.1	10	nA
		$T_A=-40^\circ C$ to $85^\circ C$		1		
$V_{OUT}$ Discharge Resistance in Shutdown		$V_{EN}=0$		300		
Thermal Shutdown Temperature	$T_{SHDN}$	$T_J$ Rising		160		
Thermal Shutdown Hysteresis	$\Delta T_{SHDN}$			15		
Output Capacitor	$C_{OUT}$	$I_{OUT}=0$ to 300mA		2.2 $\mu F$		

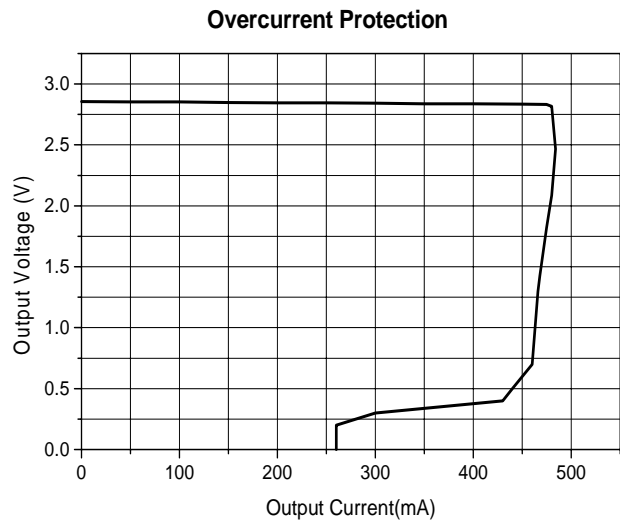
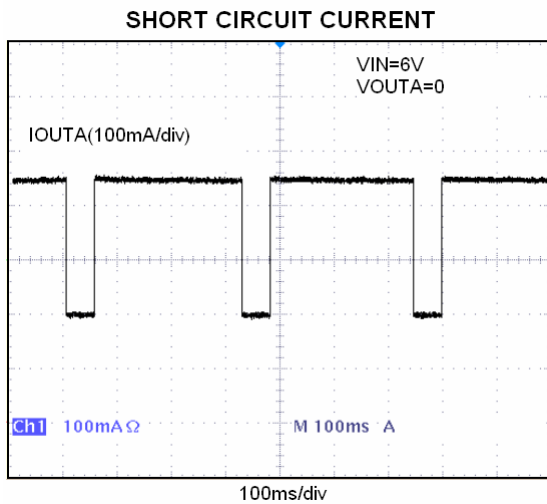
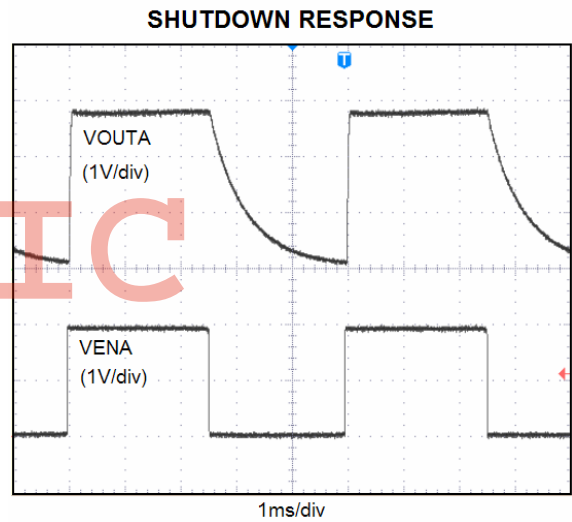
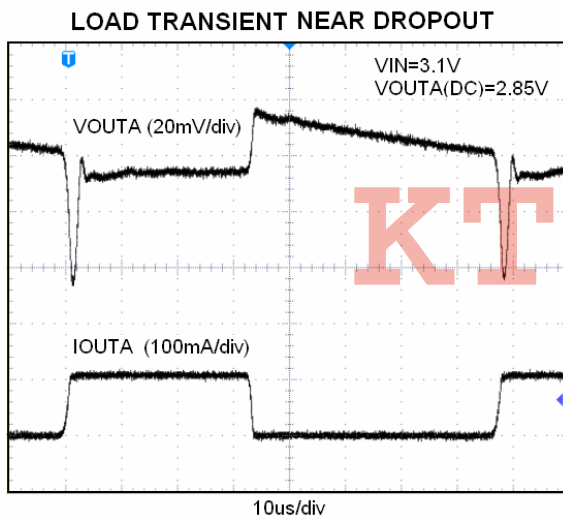
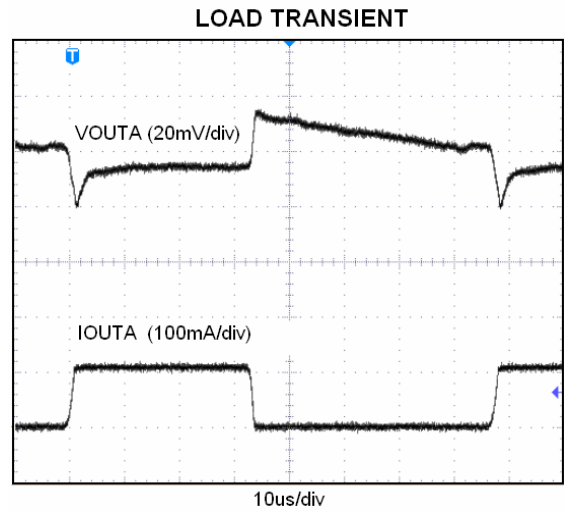
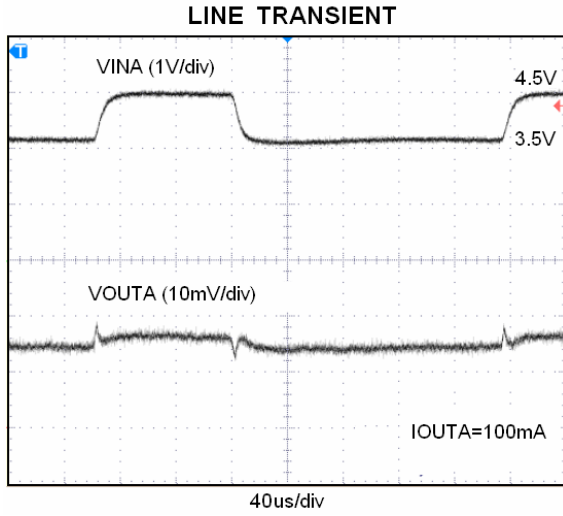
**Typical Operating Characteristics**

Unless otherwise specified,  $C_{IN}=C_{OUT}=2.2\mu F$ ,  $C_{BP}=0.01\mu F$ ,  $V_{IN}=3.8V$ ,  $V_{ENA}=V_{ENB}=V_{IN}$ ,  $I_o=10mA$ ,  $V_{OUTA}=V_{OUTB}=2.85V$ .



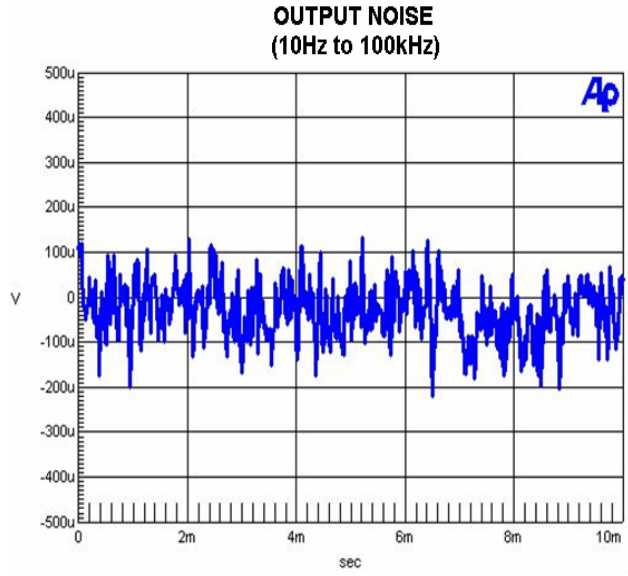
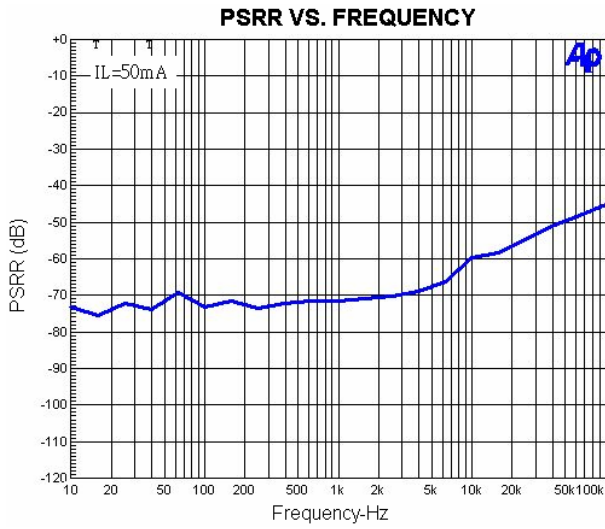
**Typical Operating Characteristics (continued)**

Unless otherwise specified,  $C_{IN}=C_{OUT}=2.2\mu F$ ,  $C_{BP}=0.01\mu F$ ,  $V_{IN}=3.8V$ ,  $V_{ENA}=V_{ENB}=V_{IN}$ ,  $I_o=10mA$ ,  $V_{OUTA}=V_{OUTB}=2.85V$ .



**Typical Operating Characteristics (continued)**

Unless otherwise specified,  $C_{IN}=C_{OUT}=2.2\mu F$ ,  $C_{BP}=0.01\mu F$ ,  $V_{IN}=3.8V$ ,  $V_{ENA}=V_{ENB}=V_{IN}$ ,  $I_o=10mA$ ,  $V_{OUTA}=V_{OUTB}=2.85V$ .



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### Application Note

The EUP7559 is a high performance, low quiescent current power management IC consisting of two  $\mu$ Cap low dropout regulators. The first regulator is capable of sourcing 300mA at output voltages from 1.5V to 3.3V. The second regulator is capable of sourcing 300mA of current at output voltages from 1.5V to 3.3V. These outputs are stable with 2.2 $\mu$ F output capacitor at any load.

### Enable A and B

The enable inputs allow for logic control of both output voltages with individual enable inputs. The EUP7559 is turned off by pulling the  $V_{EN}$  pin low, and turned on by pulling it high. If this feature is not used, the  $V_{EN}$  pin should be tied to  $V_{IN}$  to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the  $V_{EN}$  input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under  $V_{IL}$  and  $V_{IH}$ .

### External Capacitors

Like any low-dropout regulator, the EUP7559 requires external capacitors for regulator stability. The EUP7559 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

### Input Capacitor

An input capacitance of  $\approx 2.2\mu\text{F}$  or greater is required between the EUP7559 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

### Output Capacitor

The EUP7559 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (temperature characteristics X7R, X5R, Z5U, or Y5V) in 2.2 $\mu\text{F}$  to 22 $\mu\text{F}$  range with 5m $\Omega$  to 500m $\Omega$  ESR range is suitable in the EUP7559 application circuit.

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range (5m $\Omega$  to 500m $\Omega$ )

### No-Load Stability

The EUP7559 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

### Capacitor Characteristics

The EUP7559 is designed to work with ceramic capacitors on the output ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 2.2 $\mu\text{F}$  ceramic capacitor is in the range of 10m $\Omega$  to 40m $\Omega$ , which easily meets the ESR requirement for stability by the EUP7559.

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55 $^{\circ}\text{C}$  to +125 $^{\circ}\text{C}$ , will only vary the capacitance to within  $\pm 15\%$ . Most large value ceramic capacitors ( $\approx 2.2\mu\text{F}$ ) are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from 25 $^{\circ}\text{C}$  to 85 $^{\circ}\text{C}$ . Therefore, X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25 $^{\circ}\text{C}$ .

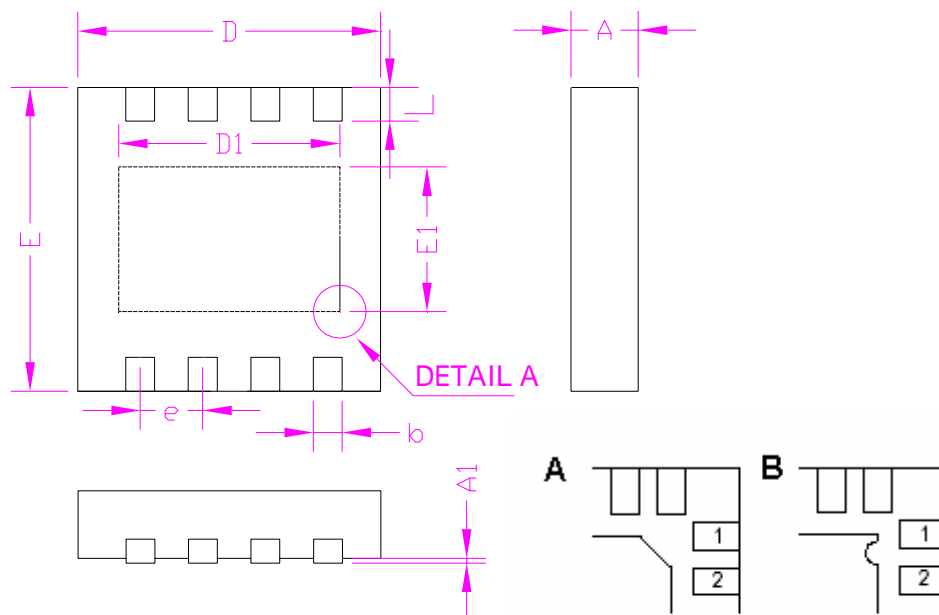
### Noise Bypass Capacitor

Connecting a 0.01 $\mu\text{F}$  capacitor between the BP pin and ground significantly reduces noise on the regulator output. This cap is connected directly to a high impedance node in the bandgap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy. The types of capacitors best suited for the noise bypass capacitor are ceramic and film.

Unlike many other LDO's, addition of a noise reduction capacitor does not effect the load transient response of the device.

Packaging Information

TDFN-8



**DETAIL A**  
Thermal Pad Option

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SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.20	0.40	0.008	0.016
D	2.90	3.10	0.114	0.122
D1	2.30		0.090	
E	2.90	3.10	0.114	0.122
E1	1.50		0.059	
e	0.65		0.026	
L	0.25	0.45	0.010	0.018