EUTECH
MICROELECTRONICS

5V/12V Synchronous Buck PWM Controller

DESCRIPTION

The EUP6514 is a high efficiency, fixed 300kHz frequency, voltage mode, synchronous PWM controller. The device drives two low cost N-channel MOSFETs and is designed to work with 5V to 12V supply voltage, providing excellent regulation for load transients.

The EUP6514 includes soft-start, frequency compensation networks nd integrates all of the controls, output adjustments, monitoring and protection functions into a single package.

A power-on-reset (POR) circuit monitors the power supply to prevent wrong logic controls. The built-in soft-start with fixed soft-start internal prevents the output voltage from overshoot as well as limiting the input current. Adjustable over-current protection monitors the voltage drop across the RDS(ON) of the lower MOSFET, with no current sense resistor required. The EUP6514 is available in 8-pins SOP package.

Pulling and holding the voltage on OPS pin below 0.1V with an open drain device shuts down the controller.

FEATURES

- Operating with 5~12V Supply Voltage
- 300 kHz Fixed Frequency Oscillator
- Built-In Feedback Compensation
  -Voltage-mode PWM Control with 0 to 100% Duty Ratio
- Fast Transient Response
  -High-Speed GM Amplifier
- Drives All Low Cost N-Channel MOSFETs
  -Adaptive Shoot-Through Protection
- Adjustable Over-Current Protection
  -Using RDS(ON) of the Low-side MOSFET
- Built-In Soft-Start
- Shutdown Control using an External
- Available in SOP-8
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- Motherboard
- Graphics Card
- High Current, up to 20A, DC-DC Converter
- Telecomm Equipments
- IA Equipments

Typical Application Circuit

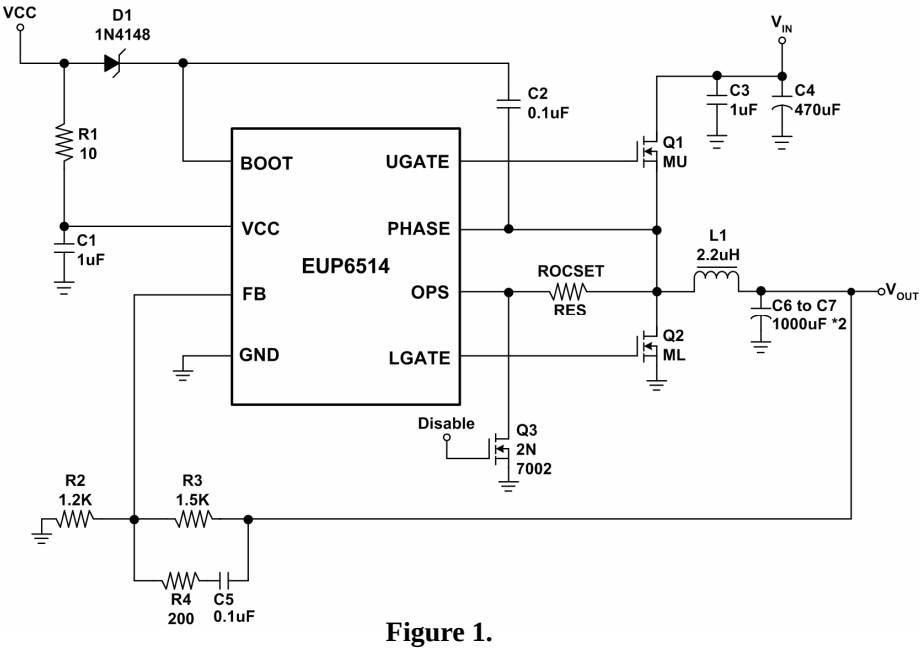
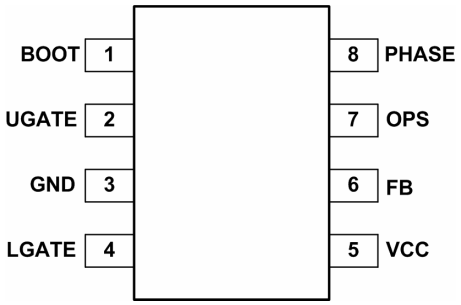


Figure 1.

Pin Configurations

Package Type	Pin Configurations
SOP-8	

Pin Description

PIN	PIN	DESCRIPTION
1	BOOT	Bootstrap supply pin for the upper gate driver. Connect the bootstrap capacitor between BOOT pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
2	UGATE	Upper gate driver output. Connect to the gate of high-side power N-Channel MOSEFT. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
3	GND	Both signal and power ground for the IC. All voltage levels are measured with respect to this pin. Ties the pin directly to the low-side MOSFET source and ground plane with the lowest impedance.
4	LGATE	Lower gate drive output. Connect to the gate of low-side power N-Channel MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
5	VCC	Connect this pin to a well-decoupled 5V or 12V bias supply. It is also the positive supply for the lower gate driver, LGATE.
6	FB	Switcher feedback voltage. This pin is the inverting input of the error amplifier. FB senses the switcher output through an external resistor divider network.
7	OPS	This pin provides multi-function of the over-current setting, UGATE turn-on POR sensing, and shut-down features. Connecting a resistor (ROCSET) between OPS and PHASE pins sets the over-current trip point. Pulling the pin to ground resets the device and all external MOSFETs are turned off allowing the output voltage power rails to float. This pin is also used to detect V_{IN} in power on stage and issues an internal POR signal.
8	PHASE	Connect this pin to the source of the upper MOSEFT and the drain of the lower MOSFET.

Block Diagram

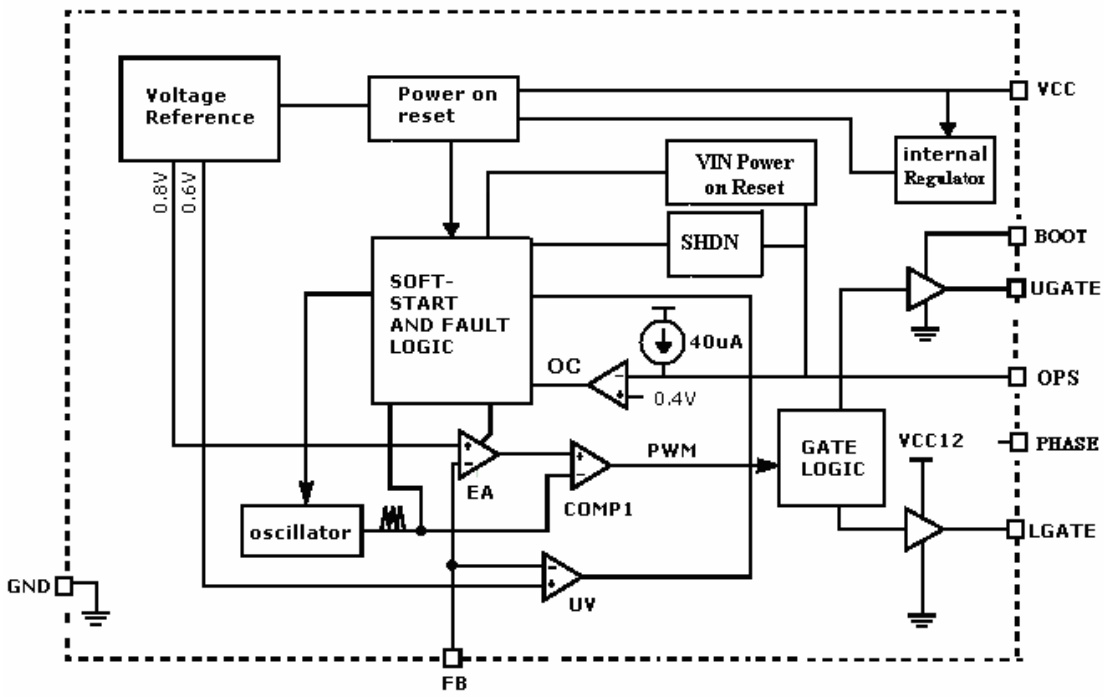


Figure 2.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP6514DIR1	SOP-8	xxxxx P6514	-40 °C to 85°C

EUP6514 □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape& Reel

Operating temperature range
I: Industry Standard

Package Type
D: SOP

Absolute Maximum Ratings

- Supply Voltage (V_{CC}) ---------- 16V
- BOOT, V_{BOOT}-V_{PHASE} ---------- 16V
- PHASE to GND
  DC ---------- -1V to 15V
- BOOT to PHASE ---------- 15V
- BOOT to GND
  DC ---------- -0.3V to V_{CC}+15V
- UGATE ---------- V_{PHASE} -0.3V to V_{BOOT} +0.3V
- LGATE ---------- GND -0.3V to V_{VCC} +0.3V
- Input, Output or I/O Voltage ---------- GND -0.3V to 7V
- Package Thermal Resistance
- SOP-8, θ_{JA} ---------- 67.9°C /W
- Junction Temperature ---------- 150°C
- Storage Temperature (Solding, 10sec.) ---------- 260°C
- ESD Susceptibility
  HBM (Human Body Mode) ---------- 2kV

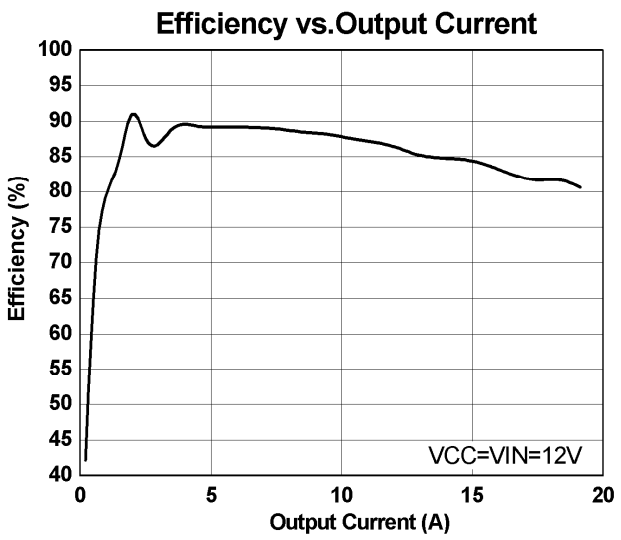
Recommended Operating Conditions

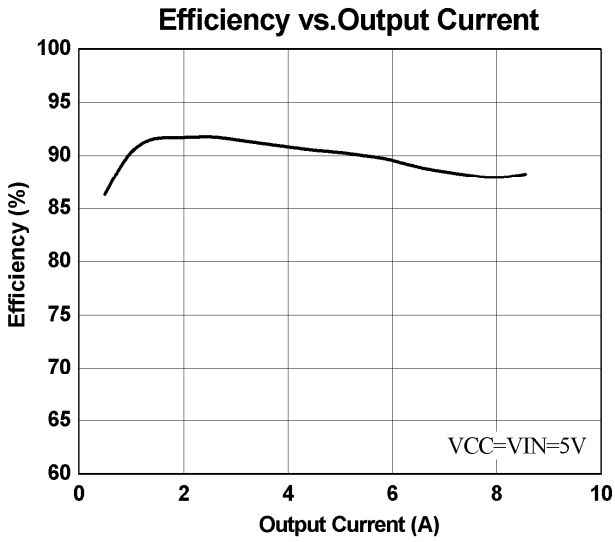
- Supply Voltage, V_{CC} ---------- 5V±5%, 12V±10%
- Ambient Temperature Range ---------- -40°C to 85°C
- Junction Temperature Range ---------- -40°C to 125°C

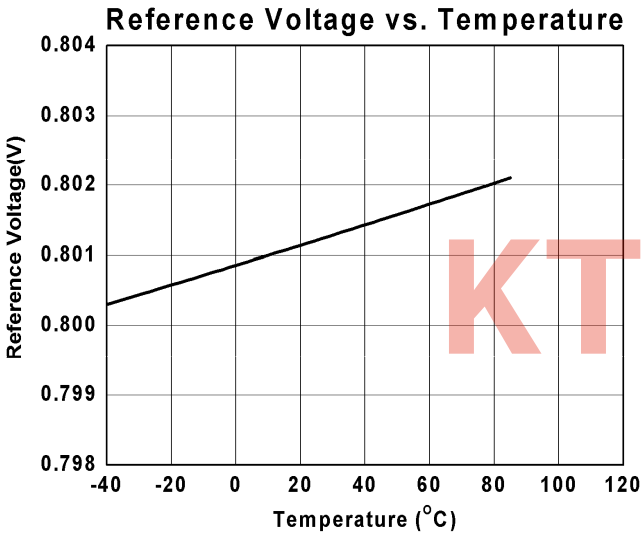
Electrical Characteristics

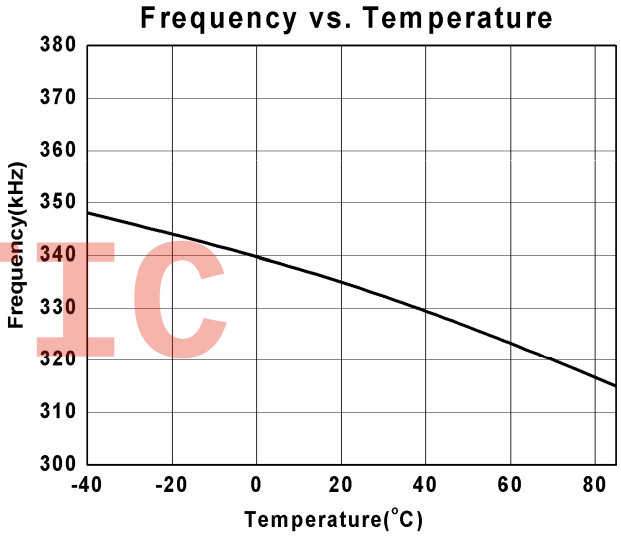
Symbol	Parameter	Conditions	EUP6514			Unit
			Min.	Typ.	Max.	
V_{CC} Supply Current						
I_{CC}	Norminal Supply Current	UGATE and LGATE open		2	5	mA
I_{CCS}	Shutdown Supply Current			1.2	2.5	mA
Power-on Reset						
V_{CCRTH}	POR Threshold	V_{CC} Rising		4.2	4.5	V
V_{CCHYS}	Hysteresis		200	400		mV
Switcher Reference						
V_{REF}	Reference Voltage	V_{CC}=12V	0.784	0.8	0.816	V
Oscillator						
f_{OSC}	Free Running Trequency	V_{CC}=12V	250	300	360	kHz
Ramp Amplitude	ΔV_{OSC}	V_{CC}=12V		1.5		V_{P-P}
Error Amplifier						
	DC Gain			80		dB
F_{P1}	First Pole Frequency			1		Hz
F_Z	Zero Frequency			1		kHz
F_{P2}	Second Pole Frequency			400		kHz
	FB Input Current				0.1	µA
PWM Controller Gate Drivers						
R_{UGATE_H}	UGATE source Rdson	V_{CC}=12V, I_{UGATE}=10mA		5	8	Ω
R_{UGATE_L}	UGATE sink Rdson	V_{UGATE}=1V, I_{UGATE}=10mA		3	6	Ω
R_{LGATE_H}	LGATE source Rdson	V_{CC}=12V, I_{LGATE}=10mA		5	8	Ω
R_{LGATE_L}	LGATE sink Rdson	V_{LGATE}=1V, I_{UGATE}=10mA		3	6	Ω
T_{DT}	Dead Time			50		ns
Protection						
UVP	Under Voltage Level	FB Falling	68	73	78	%
I_{OC}	OC Current Source	V_{PHASE}=0	35	40	45	µA
	Over-current Reference Voltage			0.4		V
T_{SS}	Soft-Start Interval			4		mS
V_{OPS_SHUT}	OPS Shutdown Threshold	Falling V_{OPS}	0.08	0.1	0.13	V

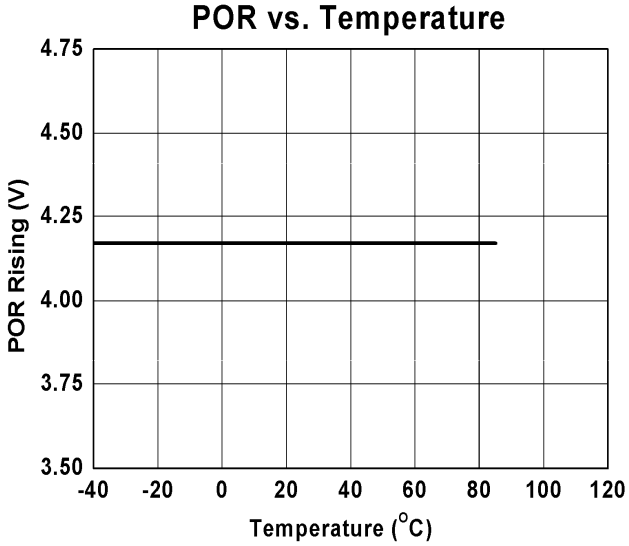
Typical Operating Characteristics

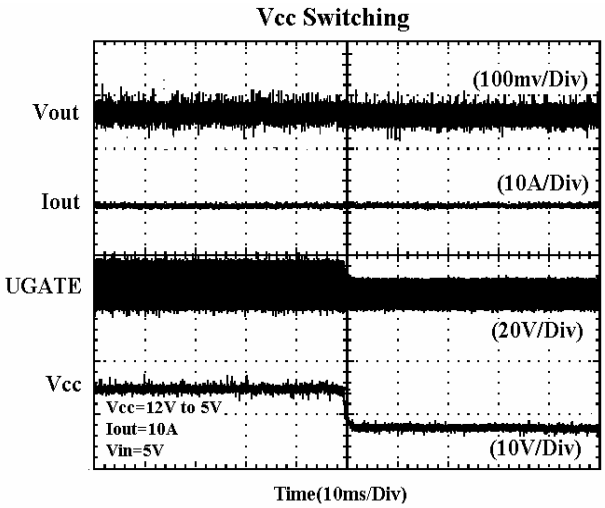






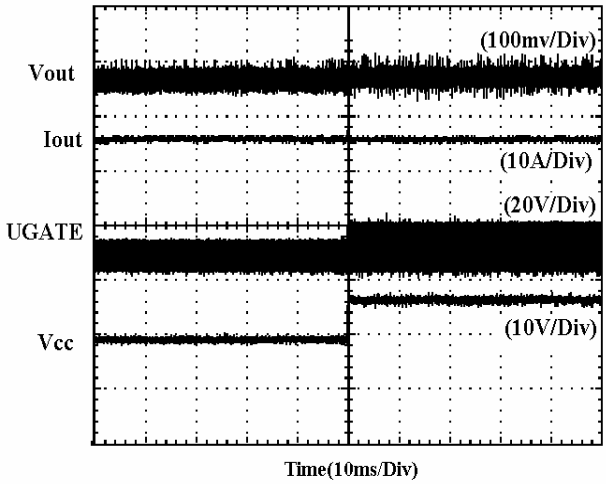




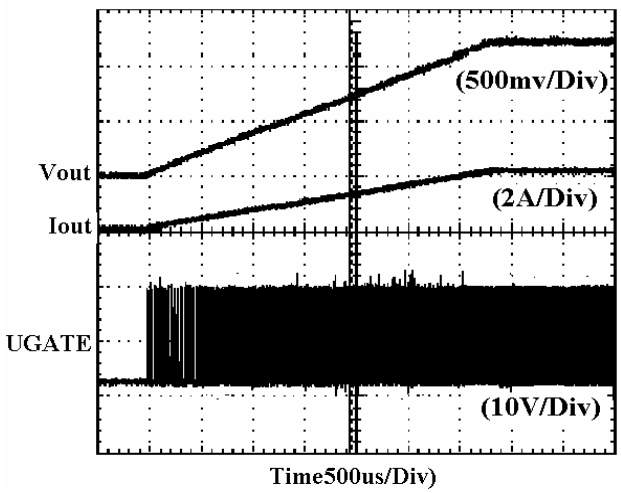


Typical Operating Characteristics (continued)

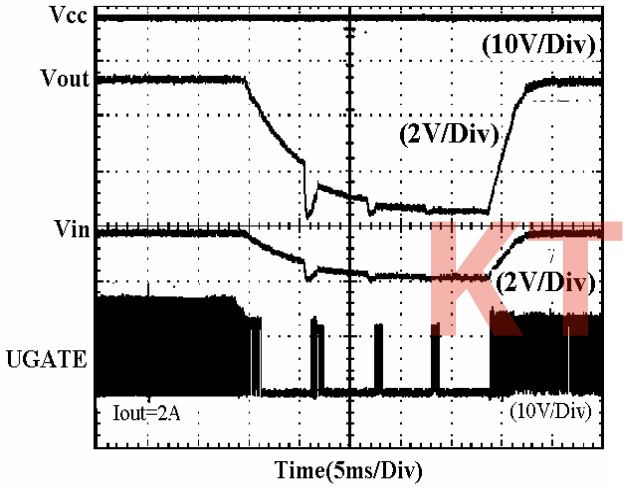
Vcc Switching



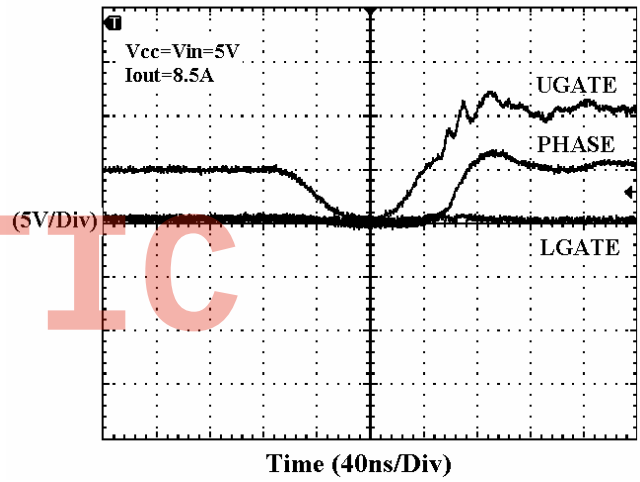
Power On



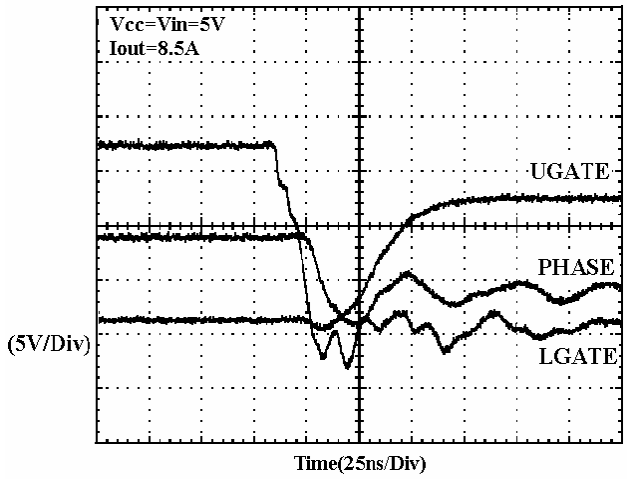
Power Off



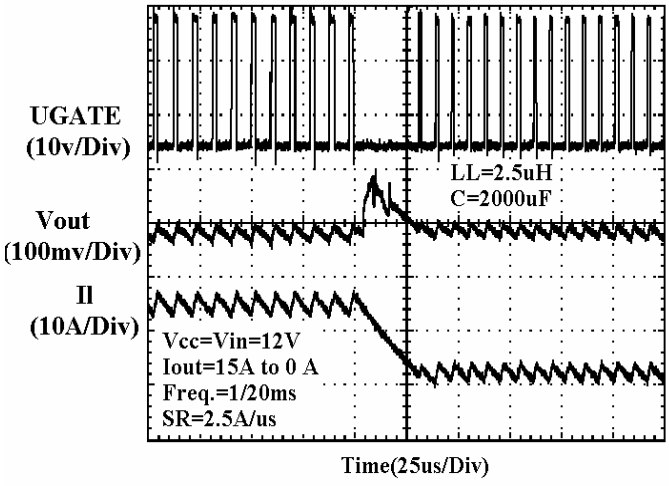
Dead Time (Rising)



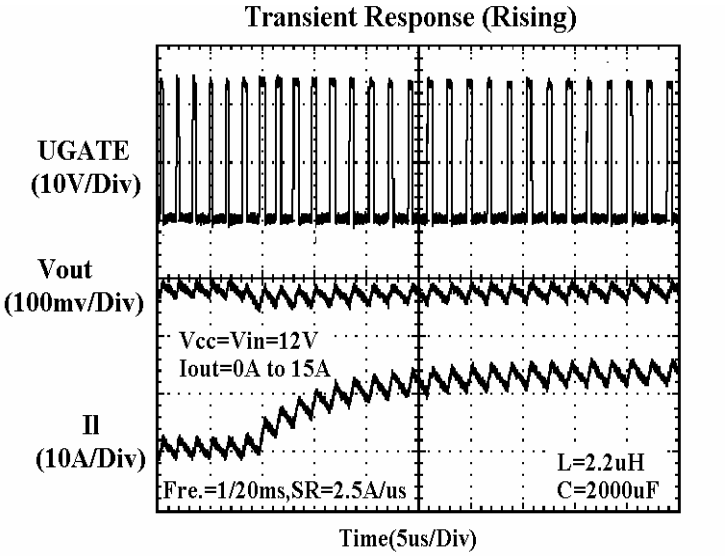
Dead Time (Falling)

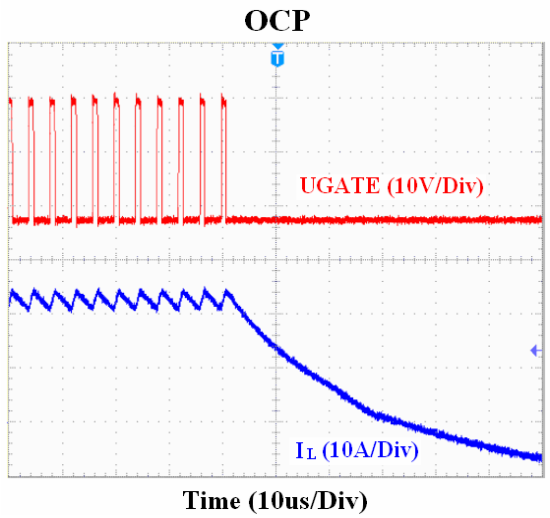


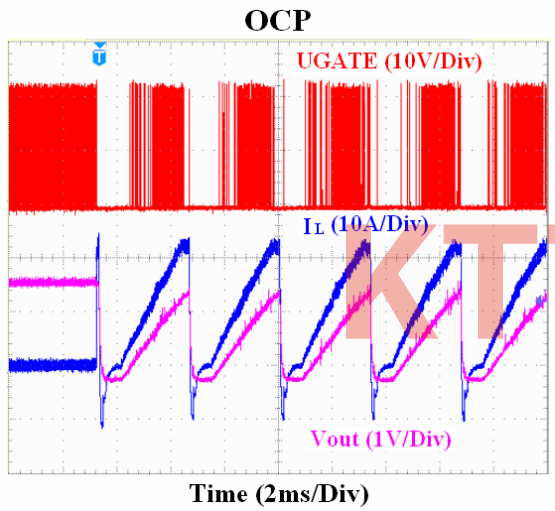
Transient Response(Falling)



Typical Operating Characteristics (continued)







Application Information

Inductor Selection

The selection of output inductor is based on the considerations of efficiency, output power and operating frequency. Low inductance value has smaller size, but results in low efficiency, large ripple current and high output ripple voltage. Generally, an inductor that limits the ripple current (ΔI_L) between 20% and 50% of output current is appropriate. Figure 3 shows the typical topology of synchronous step-down converter and its related waveforms.

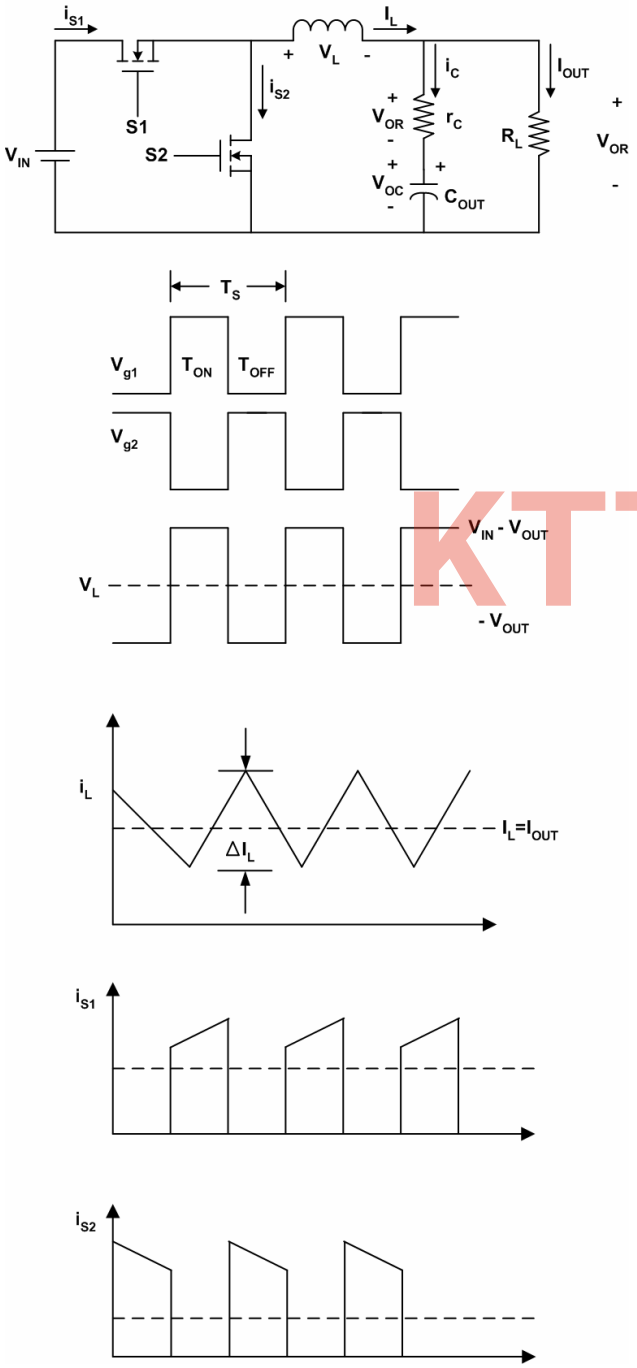


Figure 3.The waveforms of synchronous step-down converter

According to Figure 1 the ripple current of inductor can be calculated as follows :

$$V_{IN} - V_{OUT} = L\frac{\Delta I_L}{\Delta t};\ \Delta t = \frac{D}{fs};\ D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times fs \times \Delta I_L}$$

Where:

V_{IN} = Maximum input voltage

V_{OUT} = Output Voltage

Δt = S1 turn in time

ΔIL = Inductor current ripple

fs = Switching frequency

D = Duty Cycle

r_C = Equivalent series resistor of output capacitor

Output Capacitor

The selection of output capacitor depends on the output ripple voltage requirement. Practically, the output ripple voltage is a function of both capacitance value and the equivalent series resistance (ESR) r_C. Figure 4 shows the related waveforms of output capacitor.

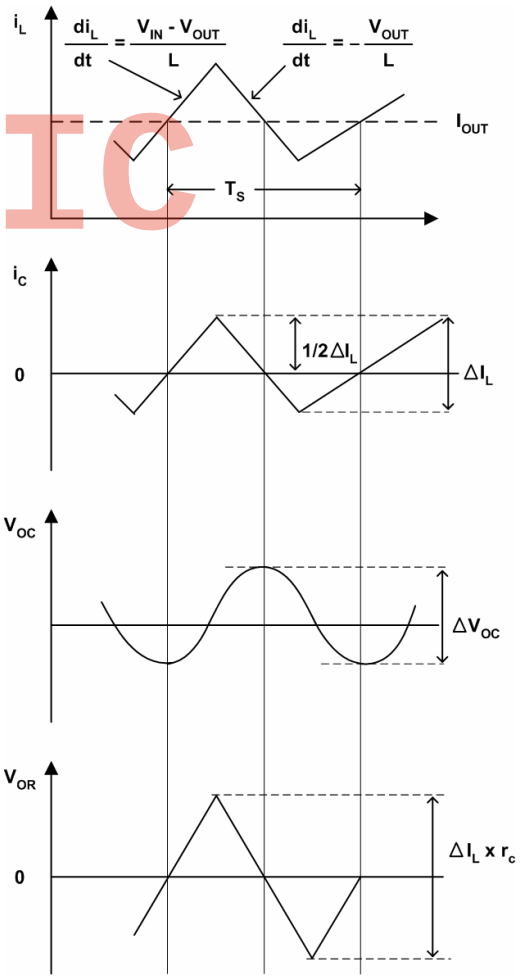


Figure 4.The related waveforms of output capacitor

The AC impedance of output capacitor at operating flows mainly through output capacitor. The output ripple voltage is described as:

$$\Delta V_{OUT} = \Delta V_{OR} + \Delta V_{OC} + V_{OC} \quad (2)$$

$$\Delta V_{OUT} = \Delta I_L \times rc + \frac{1}{C_O}\int_{t1}^{t2} ic\, dt \quad (3)$$

$$\Delta V_{OUT} = \Delta I_L \times \Delta I_L \times rc + \frac{1}{8}\frac{V_{OUT}}{C_{OL}}(1-D)T_S^2 \quad (4)$$

Where $\triangle V_{OR}$ is by ESR and ΔV_{OC} by capacitance. For electrolytic capacitor application, typically 90 to 95% of the output voltage ripple is contributed by the ESR of output capacitor. So Equation (4) could be simplified as :

$$\Delta V_{OUT} = \Delta I_L \times rc \quad (5)$$

Users could connect capacitors in parallel to get calculated ESR.

Output Capacitor

The selection of input capacitor is mainly based on its maximum ripple current capability. The buck converter draws pulsewise current from the input capacitor during the on time of S1 as shown in Figure 3. The RMS value of ripple current flowing through the input capacitor is described as:

$$Irms = I_{OUT}\sqrt{D(1-D)}\,(A) \quad (6)$$

The input capacitor must be cable of handling this ripple current. Sometime, for higher efficiency the low ESR capacitor is necessarily.

OPS (Over Current Setting, VIN_POR and Shutdown)

1.OCP

Sense the low-side MOSFET's $R_{DS(ON)}$ to set over-current trip point.

Connecting a resistor (R_{OCSET}) from this pin to the source of the upper MOSFET and the drain of the lower MOSFET sets the over-current trip point. R_{OCSET}, an internal 40µA current source, and the lower MOSFET on resistance, $R_{DS(ON)}$, set the converter over-current trip point (I_{OCSET}) according to the following equation :

$$I_{OCSET} = \frac{40\mu A \times R_{OCSET} - 0.4V}{R_{DS(ON)}\ \text{of the lower MOSFET}}$$

OPS pin function is similar to RC charging or charging or discharging circuit, so the over-current trip point is very sensitive to parasitic capacitance (ex. Shut-down MOSFET) and the duty ratio.

Below Figures say those effects. And test conditions are Rocset=15kΩ (over-current trip point=20.6A), Low-side MOSFET is IR3707.

2. VIN_POR

UGATE will continuously generate a 10kHz clock with 1% duty cycle before V_{IN} is recognized ready by detecting V_{OPS} crossing 1.5V four times (rising & falling). R_{OCSET} must be kept lower than 37.5kΩ for large R_{OCSET} will keep V_{OPS} always higher than 1.5V. Figure 6 shows the detail actions of OCP and POR. It is highly recommend-ed that R_{OCSET} be lower than 30kΩ.

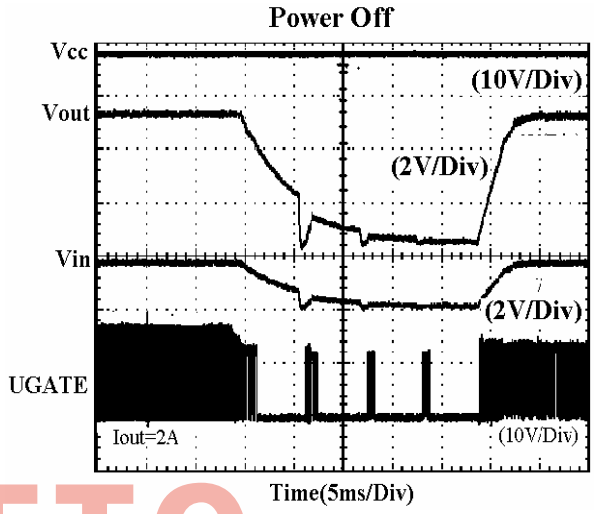


Figure 5. UV_FB trigger VIN power sensing

3. Shutdown

Pulling low the OPS pin by a small single transistor can shutdown the EUP6514 PWM controller as shown in typical application circuit.

Soft Start

A built-in soft-start is used to prevent surge current from power supply input during power on. The soft-start voltage is controlled by an internal digital counter. It clamps the ramping of reference voltage at the input of error amplifier and the pulse-width of the output driver slowly. The typical soft-start duration is 3ms.

Under Voltage Protection

The voltage at FB pin is monitored and protected against UV (under voltage). The UV threshold is the FB or FBL under 80%. UV detection has 15µs triggered delay. A hiccup restart sequence will be operating until UV state is exited.

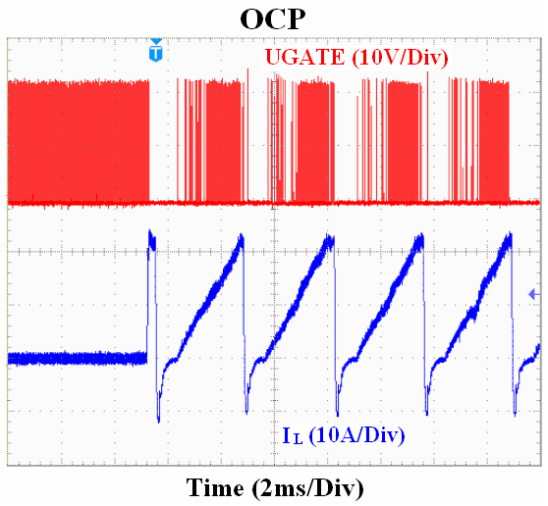


Figure 6.

PWM Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions form one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise, that results in over-voltage stress on devices. Careful component placement layout and printed circuit design can minimize the voltage spikes induced in the converter. Consider, as an example, the turn-off, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the low side MOSFET or schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes.

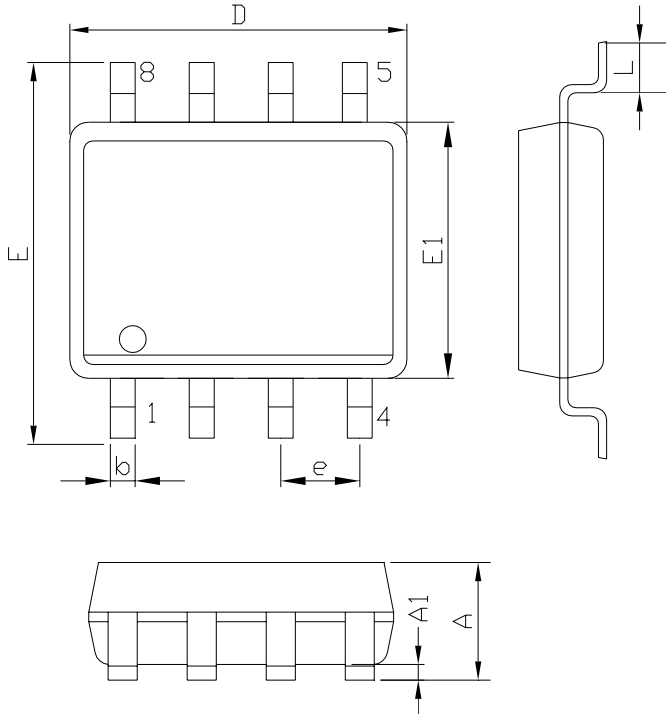
There are two sets of critical components in a DC-DC converter using the EUP6514. The switching power components are most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the PWM controller should be placed firstly. Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSEFTs and the load. Also locate the PWM controller near by MOSFETs.

A multi-layer printed circuit board is recommended.

Packaging Information

SOP-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.90		0.193	
E	5.80	6.20	0.228	0.244
E1	3.90		0.153	
L	0.40	1.27	0.016	0.050
b	0.31	0.51	0.012	0.020
e	1.27		0.050	