Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 123 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
- Non-volatile Program and Data Memories
  - 16K Byte of In-System Programmable (ISP) Program Memory Flash
    Endurance: 10,000 Write/Erase Cycles
  - 512 Bytes In-System Programmable EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 512 Bytes Internal SRAM
  - Programming Lock for Self-Programming Flash Program and EEPROM Data Security
  - Low size LIN/UART Software In-System Programmable
- Peripheral Features
  - LIN 2.1 and 1.3 Controller or 8-Bit UART
  - 8-bit Asynchronous Timer/Counter0:
    . 10-bit Clock Prescaler
    . 1 Output Compare or 8-bit PWM Channel
  - 16-bit Synchronous Timer/Counter1:
    . 10-bit Clock Prescaler
    . External Event Counter
    . 2 Output Compares Units or 16-bit PWM Channels on 2x 4 Separated Pins
  - Master/Slave SPI Serial Interface,
  - Universal Serial Interface (USI) with Start Condition Detector (Master/Slave SPI, TWI, AES, ...)
  - 10-bit ADC:
    . 11 Single Ended Channels
    . 16 Differential ADC Channel Pairs with Programmable Gain (8x or 20x)
  - On-chip Analog Comparator with Selectable Voltage Reference
  - 100µA ±6% Current Source (LIN Node Identification)
  - On-chip Temperature Sensor
  - Programmable Watchdog Timer with Separate On-chip Oscillator
- Special Microcontroller Features
  - Dynamic Clock Switching (External/Internal RC/Watchdog Clock)
  - DebugWIRE On-chip Debug (OCD) System
  - Hardware In-System Programmable (ISP) via SPI Port
  - External and Internal Interrupt Sources
  - Interrupt and Wake-up on Pin Change
  - Low Power Idle, ADC Noise Reduction, and Power-down Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Brown-out Detection Circuit
  - Internal Calibrated RC Oscillator 8MHz
  - 4-16 MHz and 32 KHz Crystal/Ceramic Resonator Oscillators
- I/O and Packages
  - 16 Programmable I/O Lines
  - 20-pin SOIC, 32-pad QFN and 20-pin TSSOP
- Operating Voltage:
  - 2.7 - 5.5V for ATtiny167
- Speed Grade:
  - 0 - 8 MHz @ 2.7 - 5.5V (Automotive Temp. Range: -40°C to +125°C)
  - 0 - 16 MHz @ 4.5 - 5.5V (Automotive Temp. Range: -40°C to +125°C)

8-bit AVR® Microcontroller with 16K Bytes In-System Programmable Flash and LIN Controller

ATtiny167 Automotive

Preliminary

Summary

7728AS-AUTO-07/08

1. Description

1.1 Part Description

The ATtiny167 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny167 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny167 provides the following features: 16K byte of In-System Programmable Flash, 512 bytes EEPROM, 512 bytes SRAM, 16 general purpose I/O lines, 32 general purpose working registers, one 8-bit Timer/Counter with compare modes, one 8-bit high speed Timer/Counter, Universal Serial Interface, a LIN controller, Internal and External Interrupts, a 4-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. The Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. The ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core. The Boot program can use any interface to download the application program in the Flash memory. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATtiny167 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny167 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

1.2 Automotive Quality Grade

The ATtiny167 have been developed and manufactured according to the most stringent requirements of the international standard ISO-TS-16949. This data sheet contains limit values extracted from the results of extensive characterization (temperature and voltage). The quality and reliability of the ATtiny167 have been verified during regular product qualification as per AEC-Q100 grade 1.
As indicated in the ordering information paragraph, the products are available in only one temperature grade as listed in Table 1-1.

Table 1-1. Temperature Grade Identification for Automotive Products

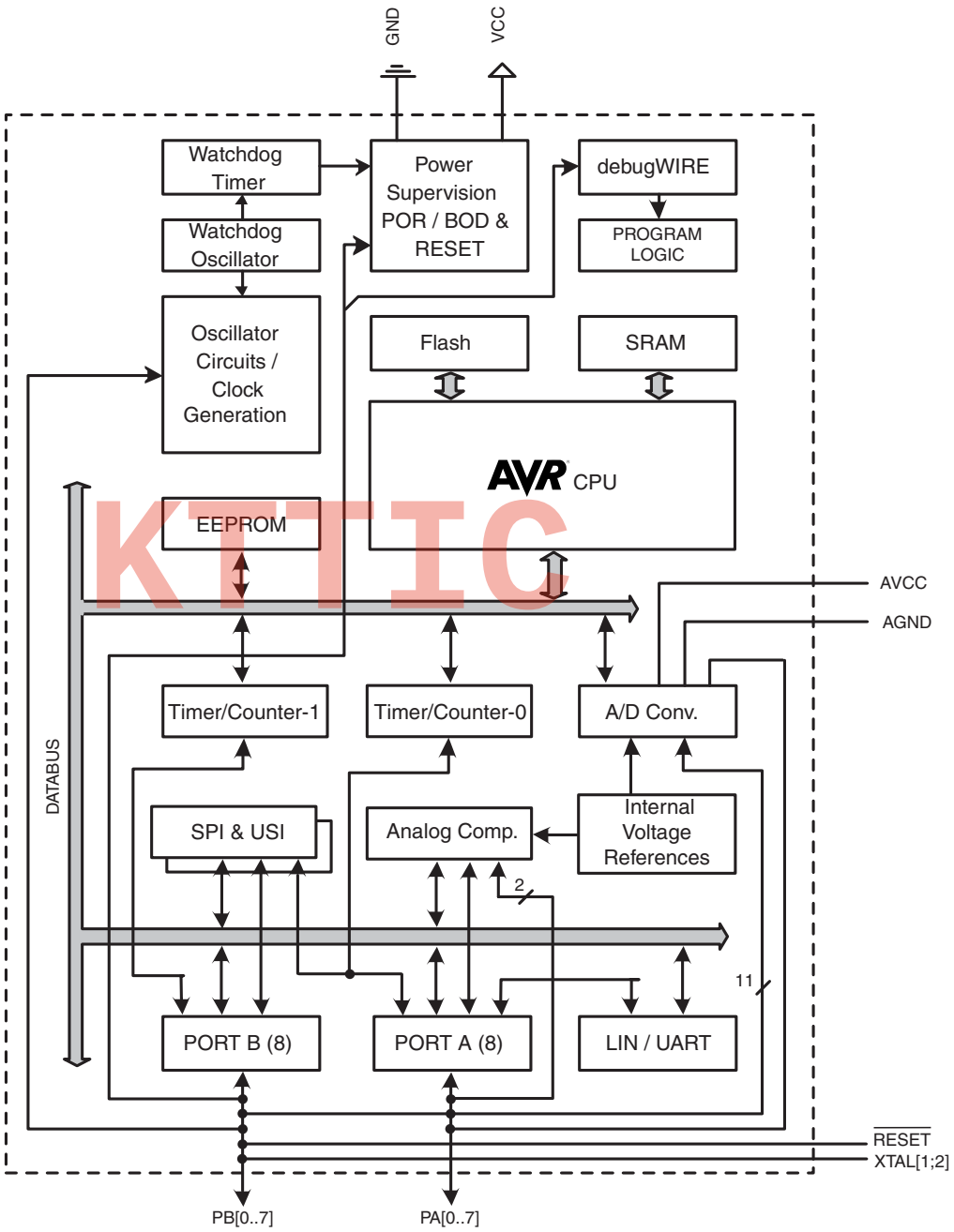
Temperature	Temperature Identifier	Comments
-40°C / +125°C	Z	Automotive Temperature Range

1.3 Disclaimer

Typical values contained in this data sheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min. and Max values will be available after the device is characterized.

1.4 Block Diagram

Figure 1-1. Block Diagram



1.5 Pin Configuration

Figure 1-2. Pinout ATtiny167 - SOIC20 & TSSOP20

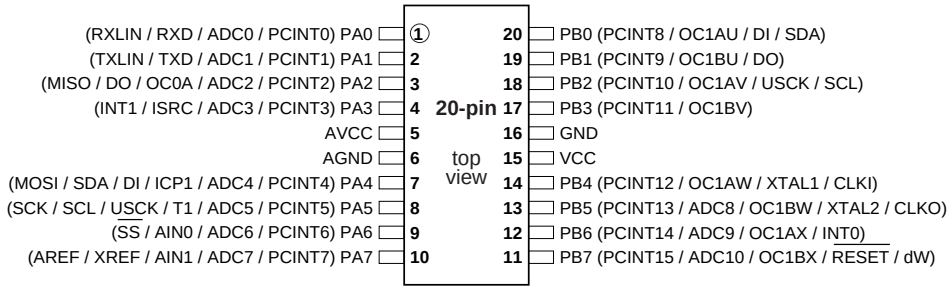
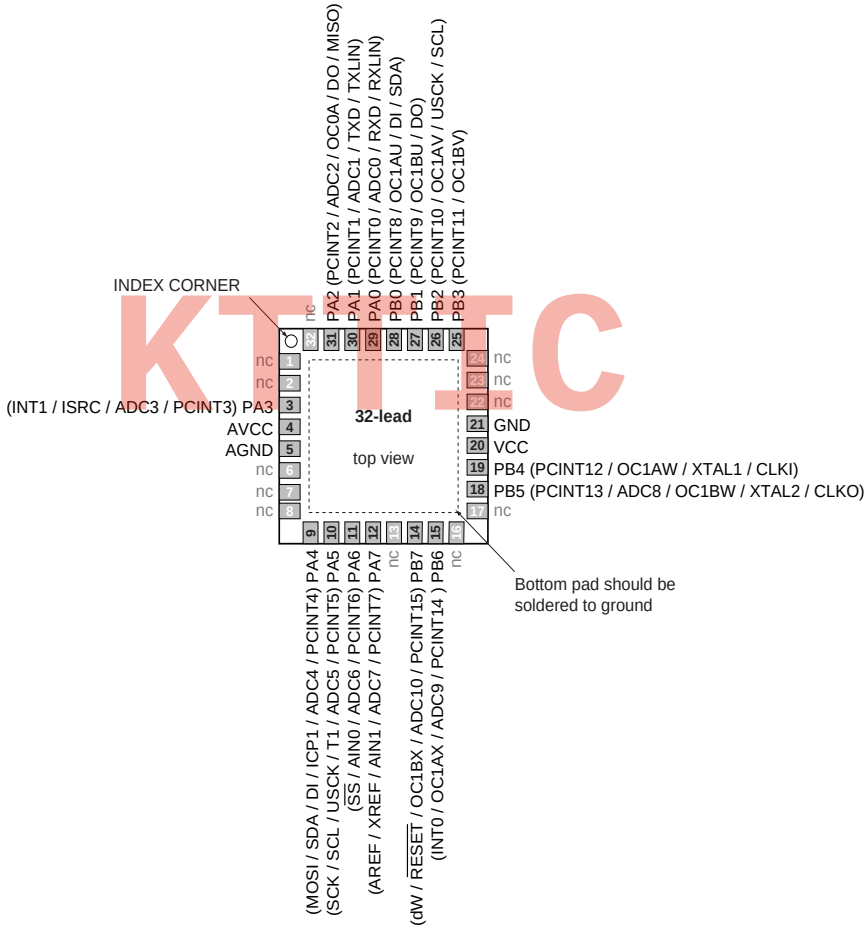


Figure 1-3. Pinout ATtiny167 - QFN32



1.6 Pin Description

1.6.1 Vcc

Supply voltage.

1.6.2 GND

Ground.

1.6.3 AVcc

Analog supply voltage.

1.6.4 AGND

Analog ground.

1.6.5 Port A (PA7..PA0)

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATtiny167 as listed on Section 9.3.3 ”Alternate Functions of Port A” on page 73.

1.6.6 Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny167 as listed on Section 9.3.4 ”Alternate Functions of Port B” on page 78.

1.7 Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

1.8 About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.