

Features

- High-performance, Low-power AVR[®] 8-bit Microcontroller
- Advanced RISC Architecture
 - 131 Powerful Instructions – Most Single-clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
 - Up to 20 MIPS Throughput at 20 MHz
- High Endurance Non-volatile Memory segments
 - 64K Bytes of In-System Self-programmable Flash program memory
 - 2K Bytes EEPROM
 - 4K Bytes Internal SRAM
 - Write/Erase cycles: 10,000 Flash/100,000 EEPROM⁽¹⁾⁽³⁾
 - Data retention: 20 years at 85°C/100 years at 25°C⁽²⁾⁽³⁾
 - Optional Boot Code Section with Independent Lock Bits
 - In-System Programming by On-chip Boot Program
 - True Read-While-Write Operation
 - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
 - Boundary-scan Capabilities According to the JTAG Standard
 - Extensive On-chip Debug Support
 - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
 - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
 - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
 - Real Time Counter with Separate Oscillator
 - Six PWM Channels
 - 8-channel, 10-bit ADC
 - Differential mode with selectable gain at 1x, 10x or 200x
 - Byte-oriented Two-wire Serial Interface
 - One Programmable Serial USART
 - Master/Slave SPI Serial Interface
 - Programmable Watchdog Timer with Separate On-chip Oscillator
 - On-chip Analog Comparator
 - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
 - Power-on Reset and Programmable Brown-out Detection
 - Internal Calibrated RC Oscillator
 - External and Internal Interrupt Sources
 - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
 - 32 Programmable I/O Lines
 - 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
- Speed Grades
 - ATmega644V: 0 - 4MHz @ 1.8 - 5.5V, 0 - 10MHz @ 2.7 - 5.5V
 - ATmega644: 0 - 10MHz @ 2.7 - 5.5V, 0 - 20MHz @ 4.5 - 5.5V
- Power Consumption at 1 MHz, 3V, 25°C for
 - Active: 240 μ A @ 1.8V, 1MHz
 - Power-down Mode: 0.1 μ A @ 1.8V

- Notes:
1. Worst case temperature. Guaranteed after last write cycle.
 2. Failure rate less than 1 ppm.
 3. Characterized through accelerated tests.



8-bit AVR[®] Microcontroller with 64K Bytes In-System Programmable Flash

ATmega644/V

Preliminary

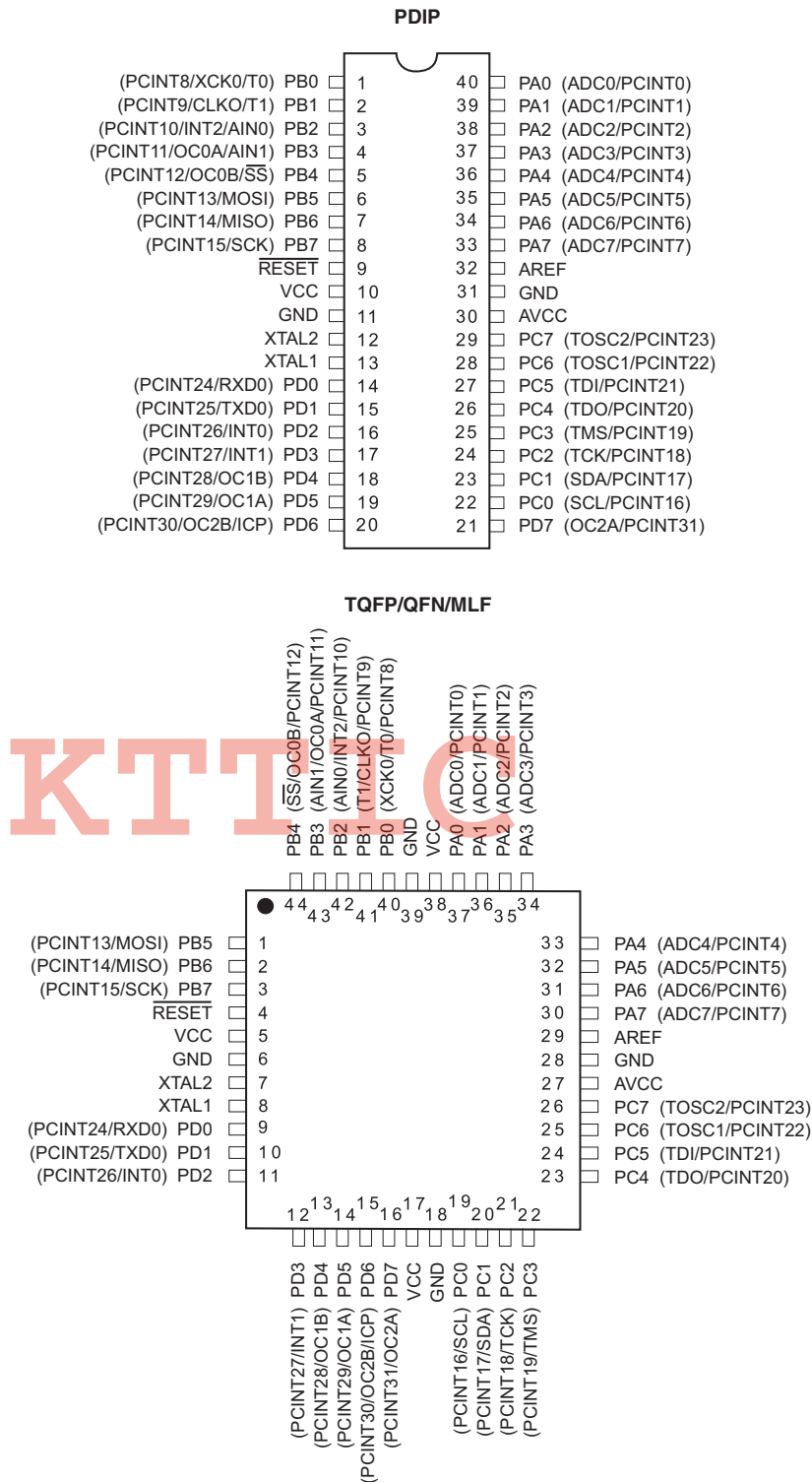
Summary

2593MS-AVR-08/07



1. Pin Configurations

Figure 1-1. Pinout ATmega644



Note: The large center pad underneath the QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

1.1 Disclaimer

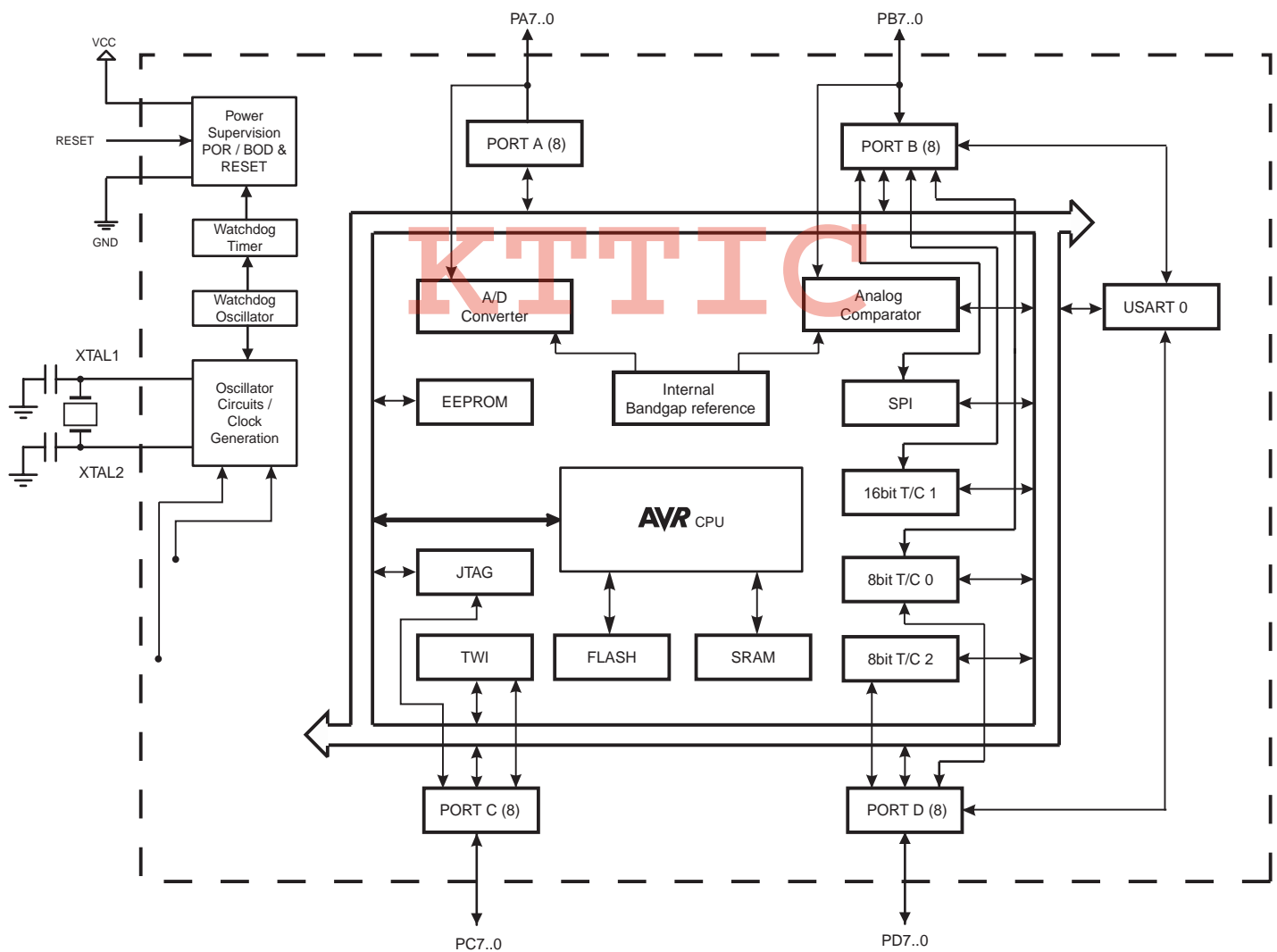
Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

2. Overview

The ATmega644 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega644 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega644 provides the following features: 64K bytes of In-System Programmable Flash with Read-While-Write capabilities, 2K bytes EEPROM, 4K bytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), three flexible Timer/Counters with compare modes and PWM, 2 USARTs, a byte oriented 2-wire Serial Interface, a 8-channel, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega644 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega644 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

2.2 Pin Descriptions

2.2.1 VCC

Digital supply voltage.

2.2.2 GND

Ground.

2.2.3 Port A (PA7:PA0)

Port A serves as analog inputs to the Analog-to-digital Converter.

Port A also serves as an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink

and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega644 as listed on [page 73](#).

2.2.4 Port B (PB7:PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega644 as listed on [page 75](#).

2.2.5 Port C (PC7:PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of the JTAG interface, along with special features of the ATmega644 as listed on [page 78](#).

2.2.6 Port D (PD7:PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega644 as listed on [page 80](#).

2.2.7 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in "System and Reset Characteristics" on [page 320](#). Shorter pulses are not guaranteed to generate a reset.

2.2.8 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.2.9 XTAL2

Output from the inverting Oscillator amplifier.

2.2.10 AVCC

AVCC is the supply voltage pin for Port F and the Analog-to-digital Converter. It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.2.11 AREF

This is the analog reference pin for the Analog-to-digital Converter.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

KTTIC

4. Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---------|----------|------------------------------------|---------|--------|-------|-------------------------------------|--------|--------|--------|---------|
| (0xFF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xFE) | Reserved | - | - | - | - | - | - | - | - | |
| (0xFD) | Reserved | - | - | - | - | - | - | - | - | |
| (0xFC) | Reserved | - | - | - | - | - | - | - | - | |
| (0xFB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xFA) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF9) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF8) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF6) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF5) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF4) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF2) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF1) | Reserved | - | - | - | - | - | - | - | - | |
| (0xF0) | Reserved | - | - | - | - | - | - | - | - | |
| (0xEF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xEE) | Reserved | - | - | - | - | - | - | - | - | |
| (0xED) | Reserved | - | - | - | - | - | - | - | - | |
| (0xEC) | Reserved | - | - | - | - | - | - | - | - | |
| (0xEB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xEA) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE9) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE8) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE6) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE5) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE4) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE2) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE1) | Reserved | - | - | - | - | - | - | - | - | |
| (0xE0) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDE) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDD) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDC) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xDA) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD9) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD8) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD6) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD5) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD4) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD2) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD1) | Reserved | - | - | - | - | - | - | - | - | |
| (0xD0) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCF) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCE) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCD) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCC) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCB) | Reserved | - | - | - | - | - | - | - | - | |
| (0xCA) | Reserved | - | - | - | - | - | - | - | - | |
| (0xC9) | Reserved | - | - | - | - | - | - | - | - | |
| (0xC8) | Reserved | - | - | - | - | - | - | - | - | |
| (0xC7) | Reserved | - | - | - | - | - | - | - | - | |
| (0xC6) | UDR0 | USART0 I/O Data Register | | | | | | | | 182 |
| (0xC5) | UBRR0H | - | - | - | - | USART0 Baud Rate Register High Byte | | | | 186/198 |
| (0xC4) | UBRR0L | USART0 Baud Rate Register Low Byte | | | | | | | | 186/198 |
| (0xC3) | Reserved | - | - | - | - | - | - | - | - | |
| (0xC2) | UCSR0C | UMSEL01 | UMSEL00 | UPM01 | UPM00 | USBS0 | UCSZ01 | UCSZ00 | UCPOL0 | 184/197 |
| (0xC1) | UCSR0B | RXCIE0 | TXCIE0 | UDRIE0 | RXEN0 | TXEN0 | UCSZ02 | RXB80 | TXB80 | 183/197 |
| (0xC0) | UCSR0A | RXC0 | TXC0 | UDRE0 | FE0 | DOR0 | UPE0 | U2X0 | MPCM0 | 182/196 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page | |
|---------|----------|--|--------|--------|--------|---------|---------|---------|---------|------|-----|
| (0xBF) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xBE) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xBD) | TWAMR | TWAM6 | TWAM5 | TWAM4 | TWAM3 | TWAM2 | TWAM1 | TWAM0 | - | 228 | |
| (0xBC) | TWCR | TWINT | TWEA | TWSTA | TWSTO | TWWC | TWEN | - | TWIE | 225 | |
| (0xBB) | TWDR | 2-wire Serial Interface Data Register | | | | | | | | | 227 |
| (0xBA) | TWAR | TWA6 | TWA5 | TWA4 | TWA3 | TWA2 | TWA1 | TWA0 | TWGCE | 228 | |
| (0xB9) | TWSR | TWS7 | TWS6 | TWS5 | TWS4 | TWS3 | - | TPSP1 | TPSP0 | 227 | |
| (0xB8) | TWBR | 2-wire Serial Interface Bit Rate Register | | | | | | | | | 225 |
| (0xB7) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xB6) | ASSR | - | EXCLK | AS2 | TCN2UB | OCR2AUB | OCR2BUB | TCR2AUB | TCR2BUB | 150 | |
| (0xB5) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xB4) | OCR2B | Timer/Counter2 Output Compare Register B | | | | | | | | | 150 |
| (0xB3) | OCR2A | Timer/Counter2 Output Compare Register A | | | | | | | | | 150 |
| (0xB2) | TCNT2 | Timer/Counter2 (8 Bit) | | | | | | | | | 150 |
| (0xB1) | TCCR2B | FOC2A | FOC2B | - | - | WGM22 | CS22 | CS21 | CS20 | 149 | |
| (0xB0) | TCCR2A | COM2A1 | COM2A0 | COM2B1 | COM2B0 | - | - | WGM21 | WGM20 | 146 | |
| (0xAF) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xAE) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xAD) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xAC) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xAB) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xAA) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xA9) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xA8) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xA7) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xA6) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xA5) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xA4) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xA3) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xA2) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xA1) | Reserved | - | - | - | - | - | - | - | - | | |
| (0xA0) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x9F) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x9E) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x9D) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x9C) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x9B) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x9A) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x99) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x98) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x97) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x96) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x95) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x94) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x93) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x92) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x91) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x90) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x8F) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x8E) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x8D) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x8C) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x8B) | OCR1BH | Timer/Counter1 - Output Compare Register B High Byte | | | | | | | | | 129 |
| (0x8A) | OCR1BL | Timer/Counter1 - Output Compare Register B Low Byte | | | | | | | | | 129 |
| (0x89) | OCR1AH | Timer/Counter1 - Output Compare Register A High Byte | | | | | | | | | 129 |
| (0x88) | OCR1AL | Timer/Counter1 - Output Compare Register A Low Byte | | | | | | | | | 129 |
| (0x87) | ICR1H | Timer/Counter1 - Input Capture Register High Byte | | | | | | | | | 130 |
| (0x86) | ICR1L | Timer/Counter1 - Input Capture Register Low Byte | | | | | | | | | 130 |
| (0x85) | TCNT1H | Timer/Counter1 - Counter Register High Byte | | | | | | | | | 129 |
| (0x84) | TCNT1L | Timer/Counter1 - Counter Register Low Byte | | | | | | | | | 129 |
| (0x83) | Reserved | - | - | - | - | - | - | - | - | | |
| (0x82) | TCCR1C | FOC1A | FOC1B | - | - | - | - | - | - | 128 | |
| (0x81) | TCCR1B | ICNC1 | ICES1 | - | WGM13 | WGM12 | CS12 | CS11 | CS10 | 127 | |
| (0x80) | TCCR1A | COM1A1 | COM1A0 | COM1B1 | COM1B0 | - | - | WGM11 | WGM10 | 125 | |
| (0x7F) | DIDR1 | - | - | - | - | - | - | AIN1D | AIN0D | 232 | |
| (0x7E) | DIDR0 | ADC7D | ADC6D | ADC5D | ADC4D | ADC3D | ADC2D | ADC1D | ADC0D | 252 | |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|-------------|----------|--|---------|---------|---------|-----------------------------------|---------|----------|---------|--------|
| (0x7D) | Reserved | - | - | - | - | - | - | - | - | |
| (0x7C) | ADMUX | REFS1 | REFS0 | ADLAR | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 | 248 |
| (0x7B) | ADCSRB | - | ACME | - | - | - | ADTS2 | ADTS1 | ADTS0 | 231 |
| (0x7A) | ADCSRA | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | 249 |
| (0x79) | ADCH | ADC Data Register High byte | | | | | | | | 251 |
| (0x78) | ADCL | ADC Data Register Low byte | | | | | | | | 251 |
| (0x77) | Reserved | - | - | - | - | - | - | - | - | |
| (0x76) | Reserved | - | - | - | - | - | - | - | - | |
| (0x75) | Reserved | - | - | - | - | - | - | - | - | |
| (0x74) | Reserved | - | - | - | - | - | - | - | - | |
| (0x73) | PCMSK3 | PCINT31 | PCINT30 | PCINT29 | PCINT28 | PCINT27 | PCINT26 | PCINT25 | PCINT24 | 63 |
| (0x72) | Reserved | - | - | - | - | - | - | - | - | |
| (0x71) | Reserved | - | - | - | - | - | - | - | - | |
| (0x70) | TIMSK2 | - | - | - | - | - | OCIE2B | OCIE2A | TOIE2 | 152 |
| (0x6F) | TIMSK1 | - | - | ICIE1 | - | - | OCIE1B | OCIE1A | TOIE1 | 130 |
| (0x6E) | TIMSK0 | - | - | - | - | - | OCIE0B | OCIE0A | TOIE0 | 101 |
| (0x6D) | PCMSK2 | PCINT23 | PCINT22 | PCINT21 | PCINT20 | PCINT19 | PCINT18 | PCINT17 | PCINT16 | 63 |
| (0x6C) | PCMSK1 | PCINT15 | PCINT14 | PCINT13 | PCINT12 | PCINT11 | PCINT10 | PCINT9 | PCINT8 | 63 |
| (0x6B) | PCMSK0 | PCINT7 | PCINT6 | PCINT5 | PCINT4 | PCINT3 | PCINT2 | PCINT1 | PCINT0 | 64 |
| (0x6A) | Reserved | - | - | - | - | - | - | - | - | |
| (0x69) | EICRA | - | - | ISC21 | ISC20 | ISC11 | ISC10 | ISC01 | ISC00 | 60 |
| (0x68) | PCICR | - | - | - | - | PCIE3 | PCIE2 | PCIE1 | PCIE0 | 62 |
| (0x67) | Reserved | - | - | - | - | - | - | - | - | |
| (0x66) | OSCCAL | Oscillator Calibration Register | | | | | | | | 37 |
| (0x65) | Reserved | - | - | - | - | - | - | - | - | |
| (0x64) | PRR | PRTWI | PRTIM2 | PRTIM0 | - | PRTIM1 | PRSPI | PRUSART0 | PRADC | 44 |
| (0x63) | Reserved | - | - | - | - | - | - | - | - | |
| (0x62) | Reserved | - | - | - | - | - | - | - | - | |
| (0x61) | CLKPR | CLKPCE | - | - | - | CLKPS3 | CLKPS2 | CLKPS1 | CLKPS0 | 37 |
| (0x60) | WDTCR | WDIF | WDIE | WDP3 | WDCE | WDE | WDP2 | WDP1 | WDP0 | 52 |
| 0x3F (0x5F) | SREG | I | T | H | S | V | N | Z | C | 11 |
| 0x3E (0x5E) | SPH | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 | 11 |
| 0x3D (0x5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 11 |
| 0x3C (0x5C) | Reserved | - | - | - | - | - | - | - | - | |
| 0x3B (0x5B) | Reserved | - | - | - | - | - | - | - | - | |
| 0x3A (0x5A) | Reserved | - | - | - | - | - | - | - | - | |
| 0x39 (0x59) | Reserved | - | - | - | - | - | - | - | - | |
| 0x38 (0x58) | Reserved | - | - | - | - | - | - | - | - | |
| 0x37 (0x57) | SPMCSR | SPMIE | RWWWSB | SIGRD | RWWWSRE | BLBSET | PGWRT | PGERS | SPMEN | 281 |
| 0x36 (0x56) | Reserved | - | - | - | - | - | - | - | - | |
| 0x35 (0x55) | MCUCR | JTD | - | - | PUD | - | - | IVSEL | IVCE | 84/267 |
| 0x34 (0x54) | MCUSR | - | - | - | JTRF | WDRF | BORF | EXTRF | PORF | 52/268 |
| 0x33 (0x53) | SMCR | - | - | - | - | SM2 | SM1 | SM0 | SE | 43 |
| 0x32 (0x52) | Reserved | - | - | - | - | - | - | - | - | |
| 0x31 (0x51) | OCDR | On-Chip Debug Register | | | | | | | | 258 |
| 0x30 (0x50) | ACSR | ACD | ACBG | ACO | ACI | ACIE | ACIC | ACIS1 | ACIS0 | 249 |
| 0x2F (0x4F) | Reserved | - | - | - | - | - | - | - | - | |
| 0x2E (0x4E) | SPDR | SPI 0 Data Register | | | | | | | | 163 |
| 0x2D (0x4D) | SPSR | SPIF | WCOL | - | - | - | - | - | SPI2X | 162 |
| 0x2C (0x4C) | SPCR | SPIE | SPE | DORD | MSTR | CPOL | CPHA | SPR1 | SPR0 | 161 |
| 0x2B (0x4B) | GPOR2 | General Purpose I/O Register 2 | | | | | | | | 25 |
| 0x2A (0x4A) | GPOR1 | General Purpose I/O Register 1 | | | | | | | | 25 |
| 0x29 (0x49) | Reserved | - | - | - | - | - | - | - | - | |
| 0x28 (0x48) | OCR0B | Timer/Counter0 Output Compare Register B | | | | | | | | 101 |
| 0x27 (0x47) | OCR0A | Timer/Counter0 Output Compare Register A | | | | | | | | 101 |
| 0x26 (0x46) | TCNT0 | Timer/Counter0 (8 Bit) | | | | | | | | 101 |
| 0x25 (0x45) | TCCR0B | FOC0A | FOC0B | - | - | WGM02 | CS02 | CS01 | CS00 | 100 |
| 0x24 (0x44) | TCCR0A | COM0A1 | COM0A0 | COM0B1 | COM0B0 | - | - | WGM01 | WGM00 | 101 |
| 0x23 (0x43) | GTCCR | TSM | - | - | - | - | - | PSRASY | PSRSYNC | 153 |
| 0x22 (0x42) | EEARH | - | - | - | - | EEPROM Address Register High Byte | | | 21 | |
| 0x21 (0x41) | EEARL | EEPROM Address Register Low Byte | | | | | | | | 21 |
| 0x20 (0x40) | EEDR | EEPROM Data Register | | | | | | | | 21 |
| 0x1F (0x3F) | EECR | - | - | EEMP1 | EEMP0 | EERIE | EEMPE | EEPE | EERE | 21 |
| 0x1E (0x3E) | GPOR0 | General Purpose I/O Register 0 | | | | | | | | 26 |
| 0x1D (0x3D) | EIMSK | - | - | - | - | - | INT2 | INT1 | INT0 | 61 |
| 0x1C (0x3C) | EIFR | - | - | - | - | - | INTF2 | INTF1 | INTF0 | 61 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|-------------|----------|--------|--------|--------|--------|--------|--------|--------|--------|------|
| 0x1B (0x3B) | PCIFR | - | - | - | - | PCIF3 | PCIF2 | PCIF1 | PCIF0 | 62 |
| 0x1A (0x3A) | Reserved | - | - | - | - | - | - | - | - | |
| 0x19 (0x39) | Reserved | - | - | - | - | - | - | - | - | |
| 0x18 (0x38) | Reserved | - | - | - | - | - | - | - | - | |
| 0x17 (0x37) | TIFR2 | - | - | - | - | - | OCF2b | OCF2A | TOV2 | 152 |
| 0x16 (0x36) | TIFR1 | - | - | ICF1 | - | - | OCF1B | OCF1A | TOV1 | 131 |
| 0x15 (0x35) | TIFR0 | - | - | - | - | - | OCF0B | OCF0A | TOV0 | 102 |
| 0x14 (0x34) | Reserved | - | - | - | - | - | - | - | - | |
| 0x13 (0x33) | Reserved | - | - | - | - | - | - | - | - | |
| 0x12 (0x32) | Reserved | - | - | - | - | - | - | - | - | |
| 0x11 (0x31) | Reserved | - | - | - | - | - | - | - | - | |
| 0x10 (0x30) | Reserved | - | - | - | - | - | - | - | - | |
| 0x0F (0x2F) | Reserved | - | - | - | - | - | - | - | - | |
| 0x0E (0x2E) | Reserved | - | - | - | - | - | - | - | - | |
| 0x0D (0x2D) | Reserved | - | - | - | - | - | - | - | - | |
| 0x0C (0x2C) | Reserved | - | - | - | - | - | - | - | - | |
| 0x0B (0x2B) | PORTD | PORTD7 | PORTD6 | PORTD5 | PORTD4 | PORTD3 | PORTD2 | PORTD1 | PORTD0 | 85 |
| 0x0A (0x2A) | DDRD | DDD7 | DDD6 | DDD5 | DDD4 | DDD3 | DDD2 | DDD1 | DDD0 | 85 |
| 0x09 (0x29) | PIND | PIND7 | PIND6 | PIND5 | PIND4 | PIND3 | PIND2 | PIND1 | PIND0 | 85 |
| 0x08 (0x28) | PORTC | PORTC7 | PORTC6 | PORTC5 | PORTC4 | PORTC3 | PORTC2 | PORTC1 | PORTC0 | 85 |
| 0x07 (0x27) | DDRC | DDC7 | DDC6 | DDC5 | DDC4 | DDC3 | DDC2 | DDC1 | DDC0 | 85 |
| 0x06 (0x26) | PINC | PINC7 | PINC6 | PINC5 | PINC4 | PINC3 | PINC2 | PINC1 | PINC0 | 85 |
| 0x05 (0x25) | PORTB | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | 84 |
| 0x04 (0x24) | DDRB | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | 84 |
| 0x03 (0x23) | PINB | PINB7 | PINB6 | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | 84 |
| 0x02 (0x22) | PORTA | PORTA7 | PORTA6 | PORTA5 | PORTA4 | PORTA3 | PORTA2 | PORTA1 | PORTA0 | 84 |
| 0x01 (0x21) | DDRA | DDA7 | DDA6 | DDA5 | DDA4 | DDA3 | DDA2 | DDA1 | DDA0 | 84 |
| 0x00 (0x20) | PINA | PINA7 | PINA6 | PINA5 | PINA4 | PINA3 | PINA2 | PINA1 | PINA0 | 84 |

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. I/O registers within the address range \$00 - \$1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
 4. When using the I/O specific commands IN and OUT, the I/O addresses \$00 - \$3F must be used. When addressing I/O registers as data space using LD and ST instructions, \$20 must be added to these addresses. The ATmega644 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from \$60 - \$FF, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

5. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|--|----------|--|---|---------------|---------|
| ARITHMETIC AND LOGIC INSTRUCTIONS | | | | | |
| ADD | Rd, Rr | Add two Registers | $Rd \leftarrow Rd + Rr$ | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | $Rd \leftarrow Rd + Rr + C$ | Z,C,N,V,H | 1 |
| ADIW | RdI,K | Add Immediate to Word | $Rdh:Rdl \leftarrow Rdh:Rdl + K$ | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | $Rd \leftarrow Rd - Rr$ | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | $Rd \leftarrow Rd - K$ | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | $Rd \leftarrow Rd - Rr - C$ | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$ | Z,C,N,V,H | 1 |
| SBIW | RdI,K | Subtract Immediate from Word | $Rdh:Rdl \leftarrow Rdh:Rdl - K$ | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | $Rd \leftarrow Rd \bullet Rr$ | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | $Rd \leftarrow Rd \bullet K$ | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | $Rd \leftarrow Rd \vee Rr$ | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | $Rd \leftarrow Rd \oplus Rr$ | Z,N,V | 1 |
| COM | Rd | One's Complement | $Rd \leftarrow 0xFF - Rd$ | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | $Rd \leftarrow 0x00 - Rd$ | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | $Rd \leftarrow Rd \bullet (0xFF - K)$ | Z,N,V | 1 |
| INC | Rd | Increment | $Rd \leftarrow Rd + 1$ | Z,N,V | 1 |
| DEC | Rd | Decrement | $Rd \leftarrow Rd - 1$ | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | $Rd \leftarrow Rd \bullet Rd$ | Z,N,V | 1 |
| CLR | Rd | Clear Register | $Rd \leftarrow Rd \oplus Rd$ | Z,N,V | 1 |
| SER | Rd | Set Register | $Rd \leftarrow 0xFF$ | None | 1 |
| MUL | Rd, Rr | Multiply Unsigned | $R1:R0 \leftarrow Rd \times Rr$ | Z,C | 2 |
| MULS | Rd, Rr | Multiply Signed | $R1:R0 \leftarrow Rd \times Rr$ | Z,C | 2 |
| MULSU | Rd, Rr | Multiply Signed with Unsigned | $R1:R0 \leftarrow Rd \times Rr$ | Z,C | 2 |
| FMUL | Rd, Rr | Fractional Multiply Unsigned | $R1:R0 \leftarrow (Rd \times Rr) \lll 1$ | Z,C | 2 |
| FMULS | Rd, Rr | Fractional Multiply Signed | $R1:R0 \leftarrow (Rd \times Rr) \lll 1$ | Z,C | 2 |
| FMULSU | Rd, Rr | Fractional Multiply Signed with Unsigned | $R1:R0 \leftarrow (Rd \times Rr) \lll 1$ | Z,C | 2 |
| BRANCH INSTRUCTIONS | | | | | |
| RJMP | k | Relative Jump | $PC \leftarrow PC + k + 1$ | None | 2 |
| IJMP | | Indirect Jump to (Z) | $PC \leftarrow Z$ | None | 2 |
| JMP | k | Direct Jump | $PC \leftarrow k$ | None | 3 |
| RCALL | k | Relative Subroutine Call | $PC \leftarrow PC + k + 1$ | None | 4 |
| ICALL | | Indirect Call to (Z) | $PC \leftarrow Z$ | None | 4 |
| CALL | k | Direct Subroutine Call | $PC \leftarrow k$ | None | 5 |
| RET | | Subroutine Return | $PC \leftarrow STACK$ | None | 5 |
| RETI | | Interrupt Return | $PC \leftarrow STACK$ | I | 5 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | $Rd - Rr$ | Z, N, V, C, H | 1 |
| CPC | Rd,Rr | Compare with Carry | $Rd - Rr - C$ | Z, N, V, C, H | 1 |
| CPI | Rd,K | Compare Register with Immediate | $Rd - K$ | Z, N, V, C, H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if (P(b)=0) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if (P(b)=1) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BREQ | k | Branch if Equal | if (Z = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N \oplus V = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N \oplus V = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |



| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|--------------------------------------|----------|------------------------------------|--|---------|---------|
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if (I = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if (I = 0) then PC ← PC + k + 1 | None | 1/2 |
| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
| SBI | P,b | Set Bit in I/O Register | I/O(P,b) ← 1 | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | I/O(P,b) ← 0 | None | 2 |
| LSL | Rd | Logical Shift Left | Rd(n+1) ← Rd(n), Rd(0) ← 0 | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | Rd(n) ← Rd(n+1), Rd(7) ← 0 | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7) | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right Through Carry | Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0) | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | Rd(n) ← Rd(n+1), n=0..6 | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | Rd(3..0) ← Rd(7..4), Rd(7..4) ← Rd(3..0) | None | 1 |
| BSET | s | Flag Set | SREG(s) ← 1 | SREG(s) | 1 |
| BCLR | s | Flag Clear | SREG(s) ← 0 | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | T ← Rr(b) | T | 1 |
| BLD | Rd, b | Bit load from T to Register | Rd(b) ← T | None | 1 |
| SEC | | Set Carry | C ← 1 | C | 1 |
| CLC | | Clear Carry | C ← 0 | C | 1 |
| SEN | | Set Negative Flag | N ← 1 | N | 1 |
| CLN | | Clear Negative Flag | N ← 0 | N | 1 |
| SEZ | | Set Zero Flag | Z ← 1 | Z | 1 |
| CLZ | | Clear Zero Flag | Z ← 0 | Z | 1 |
| SEI | | Global Interrupt Enable | I ← 1 | I | 1 |
| CLI | | Global Interrupt Disable | I ← 0 | I | 1 |
| SES | | Set Signed Test Flag | S ← 1 | S | 1 |
| CLS | | Clear Signed Test Flag | S ← 0 | S | 1 |
| SEV | | Set Twos Complement Overflow. | V ← 1 | V | 1 |
| CLV | | Clear Twos Complement Overflow | V ← 0 | V | 1 |
| SET | | Set T in SREG | T ← 1 | T | 1 |
| CLT | | Clear T in SREG | T ← 0 | T | 1 |
| SEH | | Set Half Carry Flag in SREG | H ← 1 | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | H ← 0 | H | 1 |
| DATA TRANSFER INSTRUCTIONS | | | | | |
| MOV | Rd, Rr | Move Between Registers | Rd ← Rr | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | Rd+1:Rd ← Rr+1:Rr | None | 1 |
| LDI | Rd, K | Load Immediate | Rd ← K | None | 1 |
| LD | Rd, X | Load Indirect | Rd ← (X) | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | Rd ← (X), X ← X + 1 | None | 2 |
| LD | Rd, -X | Load Indirect and Pre-Dec. | X ← X - 1, Rd ← (X) | None | 2 |
| LD | Rd, Y | Load Indirect | Rd ← (Y) | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | Rd ← (Y), Y ← Y + 1 | None | 2 |
| LD | Rd, -Y | Load Indirect and Pre-Dec. | Y ← Y - 1, Rd ← (Y) | None | 2 |
| LDD | Rd, Y+q | Load Indirect with Displacement | Rd ← (Y + q) | None | 2 |
| LD | Rd, Z | Load Indirect | Rd ← (Z) | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | Rd ← (Z), Z ← Z+1 | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | Z ← Z - 1, Rd ← (Z) | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | Rd ← (Z + q) | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | Rd ← (k) | None | 2 |
| ST | X, Rr | Store Indirect | (X) ← Rr | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | (X) ← Rr, X ← X + 1 | None | 2 |
| ST | -X, Rr | Store Indirect and Pre-Dec. | X ← X - 1, (X) ← Rr | None | 2 |
| ST | Y, Rr | Store Indirect | (Y) ← Rr | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | (Y) ← Rr, Y ← Y + 1 | None | 2 |
| ST | -Y, Rr | Store Indirect and Pre-Dec. | Y ← Y - 1, (Y) ← Rr | None | 2 |
| STD | Y+q, Rr | Store Indirect with Displacement | (Y + q) ← Rr | None | 2 |
| ST | Z, Rr | Store Indirect | (Z) ← Rr | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | (Z) ← Rr, Z ← Z + 1 | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | Z ← Z - 1, (Z) ← Rr | None | 2 |
| STD | Z+q, Rr | Store Indirect with Displacement | (Z + q) ← Rr | None | 2 |
| STS | k, Rr | Store Direct to SRAM | (k) ← Rr | None | 2 |
| LPM | | Load Program Memory | R0 ← (Z) | None | 3 |
| LPM | Rd, Z | Load Program Memory | Rd ← (Z) | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | Rd ← (Z), Z ← Z+1 | None | 3 |
| ELPM | Rd, Z | Extended Load Program Memory | Rd ← (Z) | None | 3 |
| SPM | | Store Program Memory | (Z) ← R1:R0 | None | - |
| IN | Rd, P | In Port | Rd ← P | None | 1 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---------------------------------|----------|-------------------------|--|-------|---------|
| OUT | P, Rr | Out Port | $P \leftarrow Rr$ | None | 1 |
| PUSH | Rr | Push Register on Stack | $STACK \leftarrow Rr$ | None | 2 |
| POP | Rd | Pop Register from Stack | $Rd \leftarrow STACK$ | None | 2 |
| MCU CONTROL INSTRUCTIONS | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

KTTIC

6. Ordering Information

6.1 ATmega644

| Speed (MHz) ⁽³⁾ | Power Supply | Ordering Code ⁽²⁾ | Package ⁽¹⁾ | Operational Range |
|----------------------------|--------------|---|------------------------|-------------------------------|
| 10 | 1.8 - 5.5V | ATmega644V-10AU ATmega644V-10PU ATmega644V-10MU | 44A 40P6 44M1 | Industrial (-40°C to 85°C) |
| 20 | 2.7 - 5.5V | ATmega644-20AU ATmega644-20PU ATmega644-20MU | 44A 40P6 44M1 | Industrial (-40°C to 85°C) |

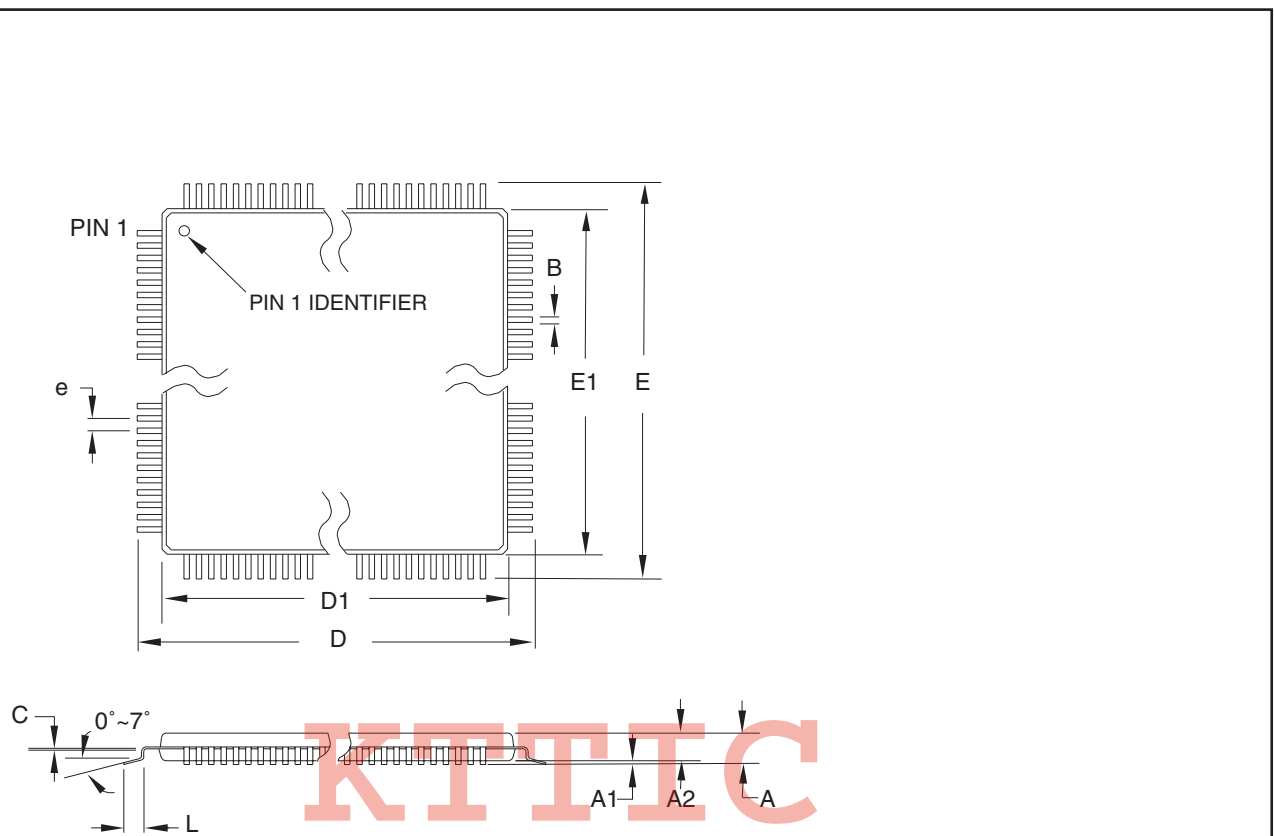
- Note:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see "[Speed Grades](#)" on page 318.

KTTIC

| Package Type | |
|--------------|---|
| 44A | 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP) |
| 40P6 | 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| 44M1 | 44-pad, 7 x 7 x 1.0 mm body, lead pitch 0.50 mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF) |

7. Packaging Information

7.1 44A



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-------|-------|--------|
| A | - | - | 1.20 | |
| A1 | 0.05 | - | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 11.75 | 12.00 | 12.25 | |
| D1 | 9.90 | 10.00 | 10.10 | Note 2 |
| E | 11.75 | 12.00 | 12.25 | |
| E1 | 9.90 | 10.00 | 10.10 | Note 2 |
| B | 0.30 | - | 0.45 | |
| C | 0.09 | - | 0.20 | |
| L | 0.45 | - | 0.75 | |
| e | 0.80 TYP | | | |

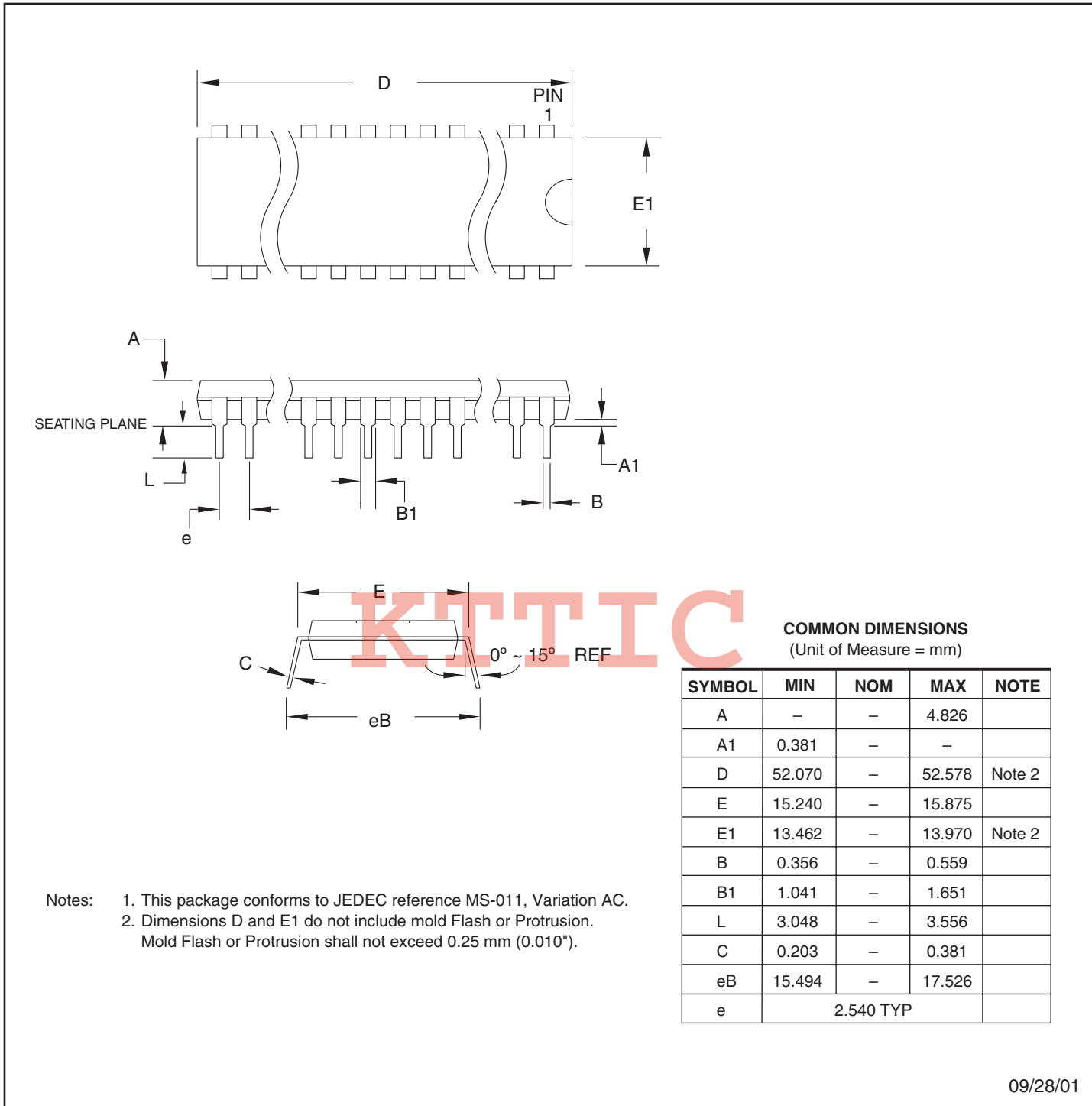
- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

| | | | |
|--|--|--------------------|-------------|
| 2325 Orchard Parkway San Jose, CA 95131 | TITLE 44A , 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | DRAWING NO. | REV. |
| | | 44A | B |



7.2 40P6



COMMON DIMENSIONS
(Unit of Measure = mm)

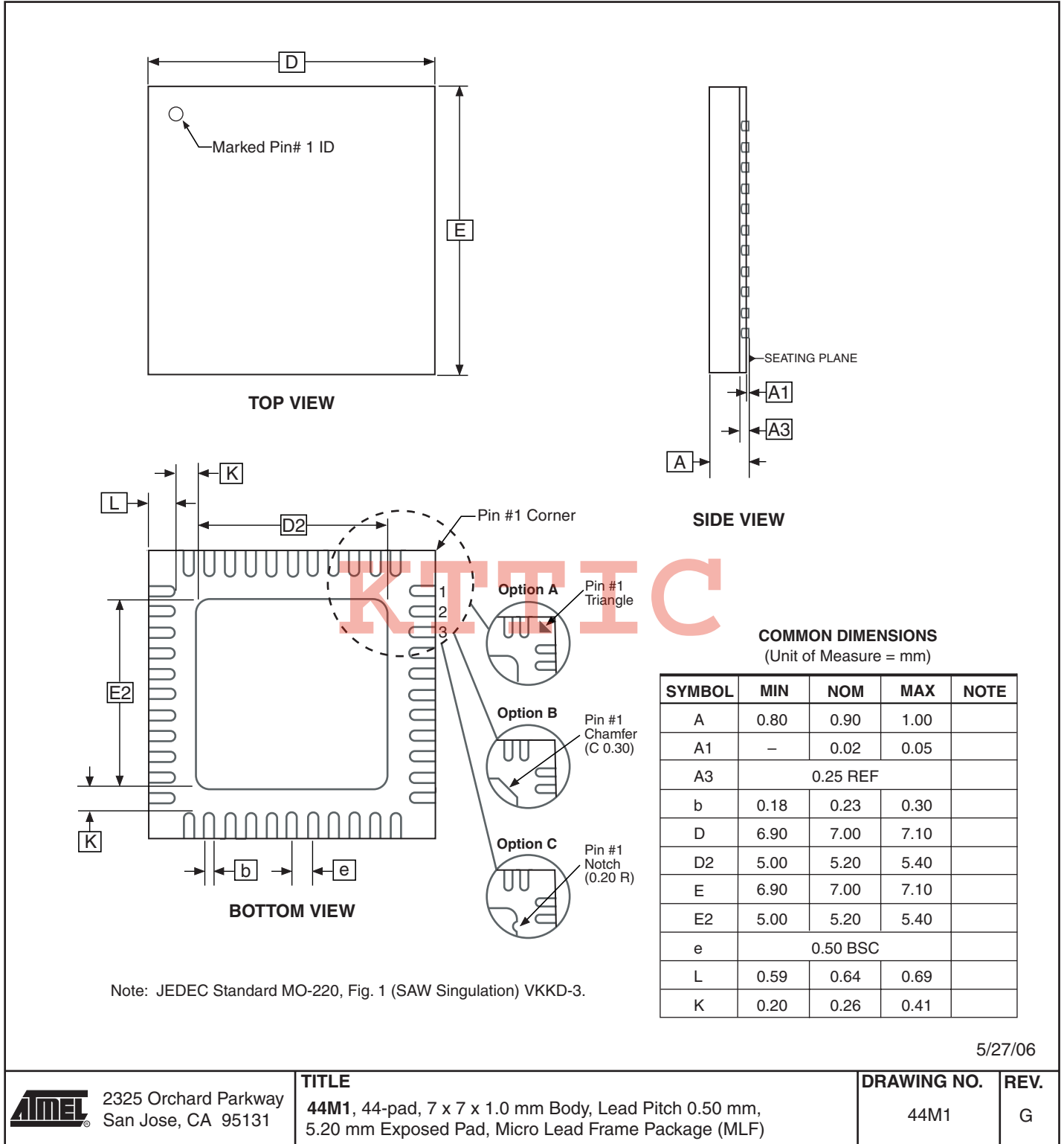
| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | - | - | 4.826 | |
| A1 | 0.381 | - | - | |
| D | 52.070 | - | 52.578 | Note 2 |
| E | 15.240 | - | 15.875 | |
| E1 | 13.462 | - | 13.970 | Note 2 |
| B | 0.356 | - | 0.559 | |
| B1 | 1.041 | - | 1.651 | |
| L | 3.048 | - | 3.556 | |
| C | 0.203 | - | 0.381 | |
| eB | 15.494 | - | 17.526 | |
| e | 2.540 TYP | | | |

Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

| | | | |
|--|--|----------------------------|------------------|
|  2325 Orchard Parkway San Jose, CA 95131 | TITLE 40P6, 40-lead (0.600"/15.24 mm Wide) Plastic Dual In-line Package (PDIP) | DRAWING NO. 40P6 | REV. B |
| | 2593MS-AVR-08/07 | | |

7.3 44M1



8. Errata

8.1 Rev. C

- **Inaccurate ADC conversion in differential mode with 200x gain.**

1. **Inaccurate ADC conversion in differential mode with 200x gain**

With AVCC < 3.6V, random conversions will be inaccurate. Typical absolute accuracy may reach 64 LSB.

Problem Fix/Workaround

None

8.2 Rev. B

Not sampled

8.3 Rev. A

- **EEPROM read from application code does not work in Lock Bit Mode 3.**

1. **EEPROM read from application code does not work in Lock Bit Mode 3**

When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

Problem Fix/Work around

Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

KTTIC

9. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

9.1 Rev. 2593M - 08/07

1. Updated "Features" on page 1.
2. Updated description in "Stack Pointer" on page 13.
3. Updated "Power-on Reset" on page 46.
4. Updated "Brown-out Detection" on page 47.
5. Updated "Internal Voltage Reference" on page 48.
6. Updated code example in "MCUCR – MCU Control Register" on page 58.
7. Added "System and Reset Characteristics" on page 320.
8. All Register Descriptions moved to the end of their respective chapters.

9.2 Rev. 2593L - 02/07

1. Updated bit description on page 153
2. Updated typos in "External Interrupts" Section 11.1.6 on page 63
3. Updated Table 24-8 on page 280
4. Updated Table 24-7 on page 280.

9.3 Rev. 2593K - 01/07

KTTIC

1. Removed the "Not recommended in new designs" notice on page 1.
2. Updated Figure 2-1 on page 3.
3. Updated "PCIFR – Pin Change Interrupt Flag Register" on page 62.
4. Updated Table 21-4 on page 248.
5. Added note to "DC Characteristics" on page 316.

9.4 Rev. 2593J - 09/06

1. Updated "Calibrated Internal RC Oscillator" on page 33.
2. Updated "Fast PWM Mode" on page 117.
3. Updated "Device Identification Register" on page 260.
4. Updated "Signature Bytes" on page 287.
5. Updated Table 13-3 on page 97, Table 13-6 on page 98, Table 14-3 on page 126, Table 14-4 on page 126, Table 14-5 on page 127, Table 15-3 on page 146, Table 15-6 on page 147 and Table 15-8 on page 148.

9.5 Rev. 2593I - 08/06

1. Updated note in "Pin Configurations" on page 2.
2. Updated Table 7-2 on page 29, Table 12-11 on page 80 and Table 24-7 on page 280.
3. Updated "Timer/Counter Prescaler" on page 145.

9.6 Rev. 2593H - 07/06

1. Updated "Fast PWM Mode" on page 117.
2. Updated Figure 14-7 on page 118.
3. Updated Table 24-7 on page 280.
4. Updated "Packaging Information" on page 362.

9.7 Rev. 2593G - 06/06

1. Updated "Calibrated Internal RC Oscillator" on page 33.
2. Updated "OSCCAL – Oscillator Calibration Register" on page 37.
3. Updated Table 26-1 on page 319.

9.8 Rev. 2593F - 04/06

1. Updated typos.
2. Updated "ADC Noise Reduction Mode" on page 40.
3. Updated "Power-down Mode" on page 40.

9.9 Rev. 2593E - 04/06

1. Updated "Calibrated Internal RC Oscillator" on page 33.

9.10 Rev. 2593D - 04/06

1. Updated "Bit 6 – ACBG: Analog Comparator Bandgap Select" on page 231.
2. Updated "Prescaling and Conversion Timing" on page 236.

9.11 Rev. 2593C - 03/06

1. Added "Not recommended in new designs".
2. Removed RAMPZ– Extended Z-pointer Register for ELPM/SPM from datasheet.
3. Updated Table 10-1 on page 55.

4. Updated code example in "Interrupt Vectors in ATmega644" on page 55.
5. Updated "Setting the Boot Loader Lock Bits by SPM" on page 276.
6. Updated "Register Summary" on page 354.

9.12 Rev. 2593B - 03/06

1. Removed the occurancy of ATmega164 and ATmega324.
2. Updated Adresses in Registers.
3. Updated "Architectural Overview" on page 9.
4. Updated SRAM sizes in "SRAM Data Memory" on page 18.
5. Updated "I/O Memory" on page 20.
6. Updated "PRR – Power Reduction Register" on page 44.
7. Updated Register bit Discription in "Register Description" on page 146.
8. Updated Note in "Overview of the TWI Module" on page 206.
9. Updated Feauters in "Analog-to-digital Converter" on page 233.
10. Changed name from "SFIOR" to "ADCSRB" in "Starting a Conversion" on page 235, in "Bit 5 – ADATE: ADC Auto Trigger Enable" on page 250 and "Bit 7, 5:3 – Res: Reserved Bits" on page 251.
11. Updated "Signature Bytes" on page 287.
12. Updated "DC Characteristics" on page 316.
13. Updated "Typical Characteristics" on page 326.
14. Updated Example in "Supply Current of IO modules" on page 331.
15. Updated "Register Summary" on page 354.
16. Updated Figure 6-2 on page 18 and Figure 21-1 on page 234.
17. Updated "Errata" on page 365.
18. Updated Table 9-1 on page 47, Table 9-4 on page 51, Table 10-1 on page 55, Table 23-1 on page 260, Table 25-7 on page 287, Table 25-15 on page 299, Table 26-6 on page 322, Table 27-1 on page 331, Table 27-2 on page 332.

9.13 Rev. 2593A-06/05

1. Initial revision.



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