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Features

- 3.0V to 5.5V Operating Range
- Lowest Power in It Class
- Advanced Low-voltage, Zero-power, Electrically Erasable Programmable Logic Device
- “Zero” Standby Power (25 µA Maximum) (Input Transition Detection)
- Low-voltage Equivalent of ATF22V10CZ
- Ideal for Battery Powered Systems
- CMOS- and TTL-compatible Inputs and Outputs
- Inputs are 5V Tolerant
- Latch Feature Hold Inputs to Previous Logic States
- EE Technology
  - Reprogrammable
  - 100% Tested
- High-reliability CMOS Process
  - 20-year Data Retention
  - 10,000 Erase/Write Cycles
  - 2,000V ESD Protection
  - 200 mA Latch-up Immunity
- Commercial and Industrial Temperature Ranges
- Dual Inline and Surface Mount Standard Pinouts
- Green Package Options (Pb/Halide-free/RoHS Compliant) Available

High-performance EE PLD

ATF22LV10CZ
ATF22LV10CQZ

1. Description

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The ATF22LV10CZ/CQZ is a high-performance CMOS (electrically erasable) programmable logic device (PLD) that utilizes Atmel’s proven electrically erasable Flash memory technology and provides 25 ns speed with standby current of 25 µA maximum. All speed ranges are specified over the 3.0V to 5.5V range for industrial and commercial temperature ranges.

The ATF22LV10CZ/CQZ provides a low-voltage and edge-sensing “zero” power CMOS PLD solution with “zero” standby power (5 µA typical). The ATF22LV10CZ/CQZ powers down automatically to the zero power mode through Atmel’s patented Input Transition Detection (ITD) circuitry when the device is idle. The ATF22LV10CZ/CQZ is capable of operating at supply voltages down to 3.0V. Pin “keeper” circuits on input and output pins hold pins to their previous logic levels when idle, which eliminate static power consumed by pull-up resistors. The “CQZ” combines this low high-frequency ICC of the “Q” design with the “Z” feature.

The ATF22LV10CZ/CQZ macrocell incorporates a variable product term architecture. Each output is allocated from 8 to 16 product terms which allows highly complex logic functions to be realized. Two additional product terms are included to provide synchronous reset and asynchronous reset. These additional product terms are common to all 10 registers and are automatically cleared upon power-up. Register Preload simplifies testing. A security fuse prevents unauthorized copying of programmed fuse patterns.

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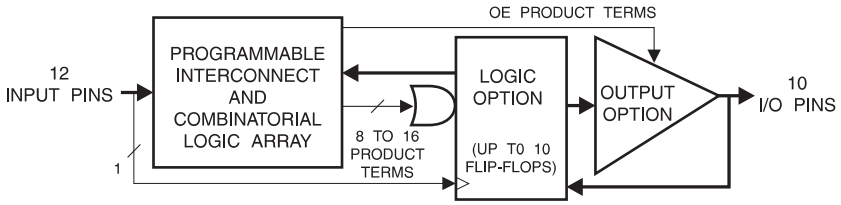
Figure 1-1. Block Diagram



2. Pin Configurations

Table 2-1. Pin Configurations (All Pinouts Top View)

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bi-directional Buffers
GND	Ground
VCC	(3 to 5.5V) Supply

Figure 2-1. TSSOP

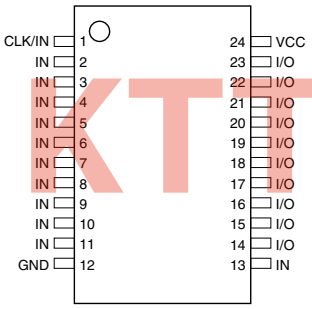
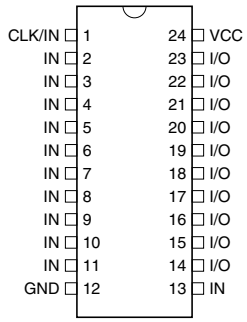
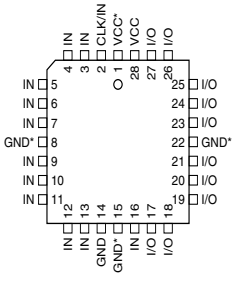


Figure 2-2. DIP/SOIC



Note: TSSOP is the smallest package of SPLD offering.

Figure 2-3. PLCC



Note: For PLCC, pins 1, 8, 15, and 22 can be left unconnected. For superior performance, connect VCC to pin 1 and GND to pins 8, 15, and 22.

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3. Absolute Maximum Ratings*

Temperature under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground during Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

4. DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3.0V - 5.5V	3.0V - 5.5V

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4.1 DC Characteristics

Symbol	Parameter	Condition[2]			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$ (Max)					-10.0	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \le V_{IN} \le V_{CC}$					10.0	µA
I_{CC}	Clocked Power Supply Current	V_{CC} = Max Outputs Open, f = 15 MHz	CZ-25	Com.		50.0	85.0	mA
			CZ-25	Ind.		55.0	90.0	mA
			CQZ-30	Com.		18.0	50.0	mA
			CQZ-30	Ind.		19.0	60.0	mA
I_{SB}	Power Supply Current, Standby	V_{CC} = Max V_{IN} = Max Outputs Open	CZ-25	Com.		3.0	25.0	µA
			CZ-25	Ind.		4.0	50.0	µA
			CQZ-30	Com.		3.0	25.0	µA
			CQZ-30	Ind.		4.0	50.0	µA
I_{OS}[1]	Output Short Circuit Current	V_{OUT} = 0.5V					-130.0	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min, I_{OL} = 16 mA					0.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = Min, I_{OH} = -2.0 mA			2.4			V
V_{OH}	Output High Voltage	I_{OH} = -100 µA			V_{CC} - 0.2V			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

2. For DC characterization, the test condition of V_{CC} = Max corresponds to 3.6V.

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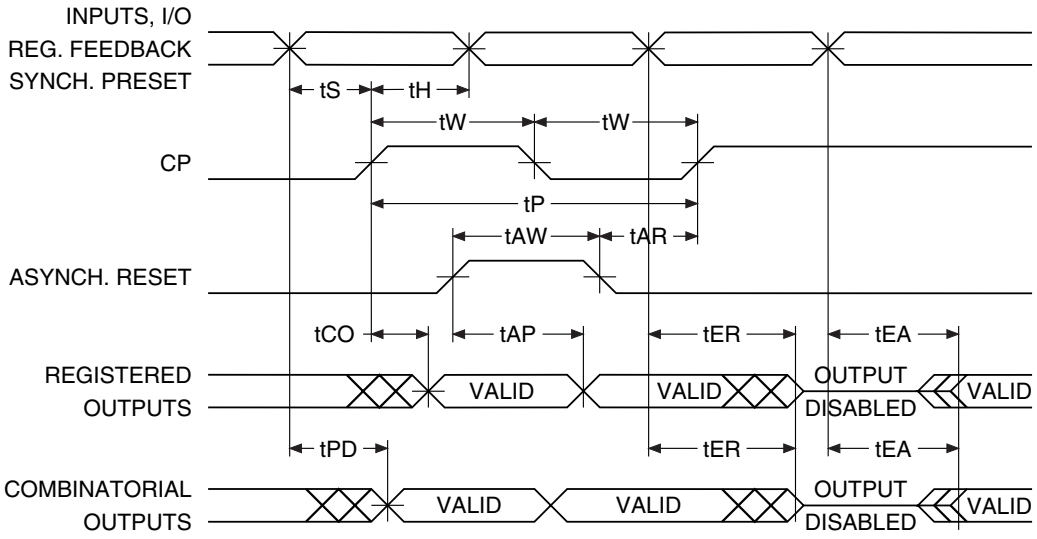
4.2 AC Waveforms



4.3 AC Characteristics[1]

Symbol	Parameter	-25		-30		Units
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-registered Output	3.0	25.0	10.0	30.0	ns
t_{CF}	Clock to Feedback		13.0	10.0	15.0	ns
t_{CO}	Clock to Output	2.0	15.0	4.0	20.0	ns
t_S	Input or Feedback Setup Time	15.0		18.0		ns
t_H	Input Hold Time	0		0		ns
t_P	Clock Period	25.0		30.0		ns
t_W	Clock Width	12.5		15.0		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$ Internal Feedback $1/(t_S + t_{CF})$ No Feedback $1/(t_P)$	33.3 35.7 40.0			25.0 30.0 33.3	MHz MHz MHz
t_{EA}	Input to Output Enable	3.0	25.0	10.0	30.0	ns
t_{ER}	Input to Output Disable	3.0	25.0	10.0	30.0	ns
t_{AP}	Input or I/O to Asynchronous Reset of Register	3.0	25.0	10.0	3.0	ns
t_{SP}	Setup Time, Synchronous Preset	15.0		20.0		ns
t_{AW}	Asynchronous Reset Width	25.0		30.0		ns
t_{AR}	Asynchronous Reset Recovery Time	25.0		30.0		ns
t_{SPR}	Synchronous Preset to Clock Recovery Time	15.0		20.0		ns

Note: 1. See ordering information for valid part numbers.

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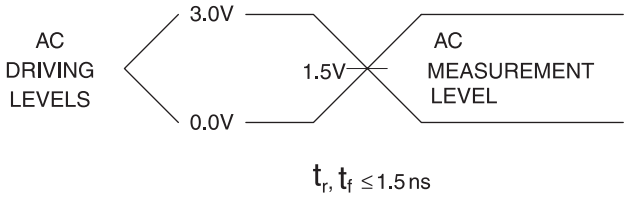
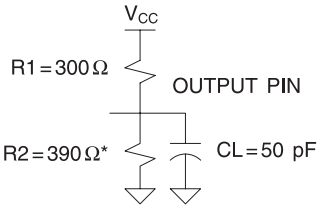
4.4 Input Test Waveforms

4.4.1 Input Test Waveforms and Measurement Levels



$t_r, t_f \leq 1.5$ ns

4.4.2 Output Test Loads



Note: Similar competitors devices are specified with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible device specification conditions.

4.5 Pin Capacitance

Table 4-1. Pin Capacitance (f = 1 MHz, T = 25°C[1])

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
$C_{I/O}$	6	8	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

4.6 Power-up Reset

The registers in the ATF22LV10CZ/CQZ are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic and start below 0.7V.
2. The clock must remain stable during T_{PR}.
3. After T_{PR}, all input and feedback setup times must be met before driving the clock pin high.

4.7 Preload of Register Outputs

The ATF22LV10CZ/CQZ's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file

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with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

5. Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

6. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22LV10CZ/CQZ fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

7. Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See CMOS PLD Programming Hardware & Software Support for information on software/ programming.

Table 7-1. Programming/Erasing

Parameter	Description	Typ	Max	Units
T_{PR}	Power-up Reset Time	600	1000	ns
V_{RST}	Power-up Reset Voltage	2.3	2.7	V

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8. Input and I/O Pin Keepers

All ATF22LV10CZ/CQZ family members have internal input and I/O pin-keeper circuits. Therefore, whenever inputs or I/Os are not being driven externally, they will maintain their last driven state. This ensures that all logic array inputs and device outputs are at known states. These are relatively weak active circuits that can be easily overridden by TTL-compatible drivers (see input and I/O diagrams below).

Figure 8-1. Input Diagram

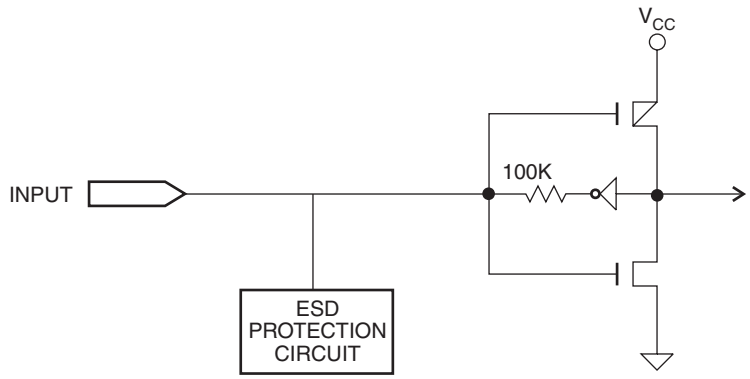

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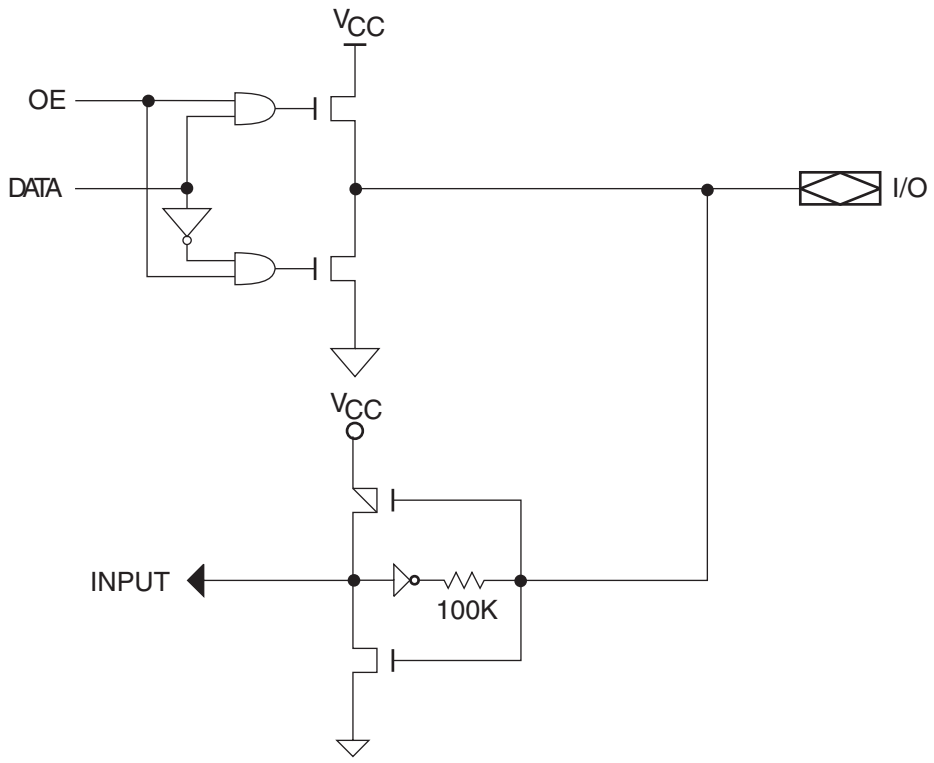
Figure 8-2. I/O Diagram



9. Functional Logic Diagram Description

The Functional Logic Diagram describes the ATF22LV10CZ/CQZ architecture.

The ATF22LV10CZ/CQZ has 12 inputs and 10 I/O macrocells. Each macrocell can be configured into one of four output configurations: active high/low or registered/combinatorial. The universal architecture of the ATF22LV10CZ/CQZ can be programmed to emulate most 24-pin PAL devices.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF22LV10CZ/CQZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

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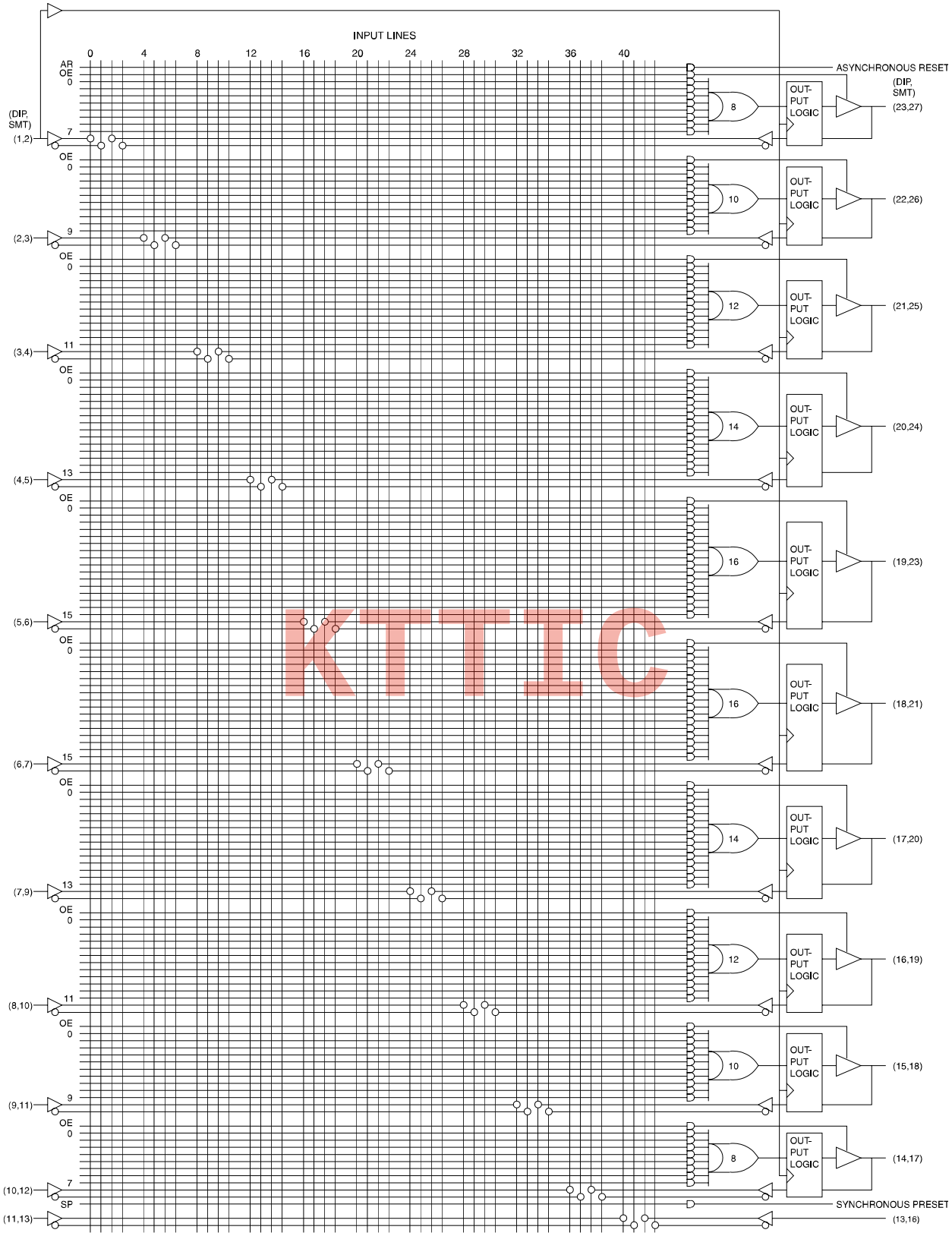
Figure 9-1. Functional Logic Diagram ATF22LV10CZ/CQZ



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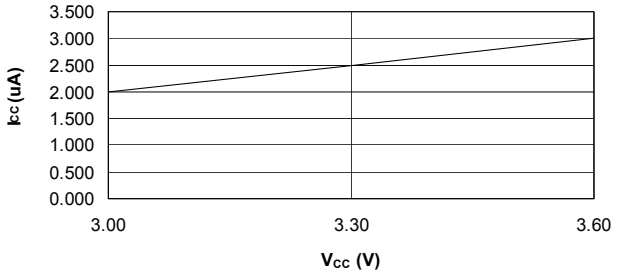
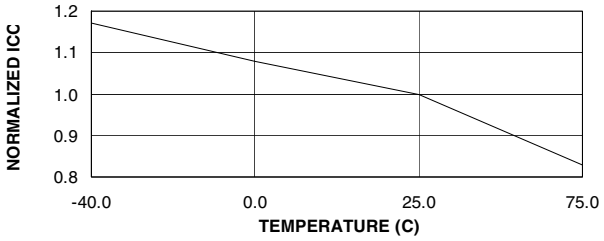
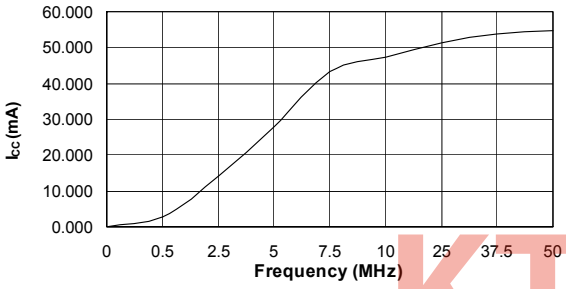
ATF22LV10CZ/CQZ STANDBY CURRENT VS. SUPPLY VOLTAGE (T_A = 25°C)



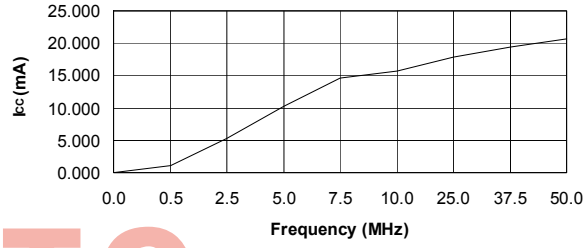
NORMALIZED I_{CC} VS. TEMP



ATF22LV10CZ SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 3.3V, T_A = 25°C)



ATF22LV10CQZ SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 3.3V, T_A = 25°C)



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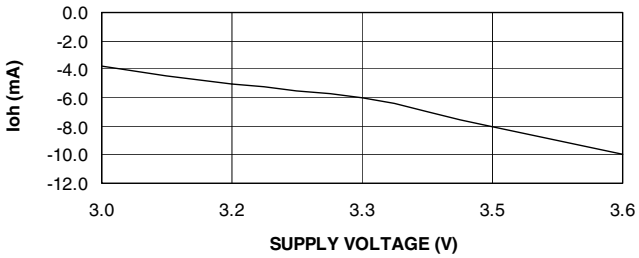
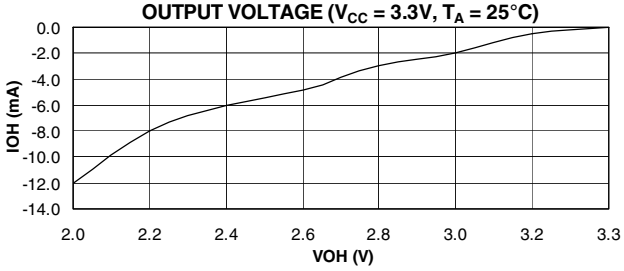
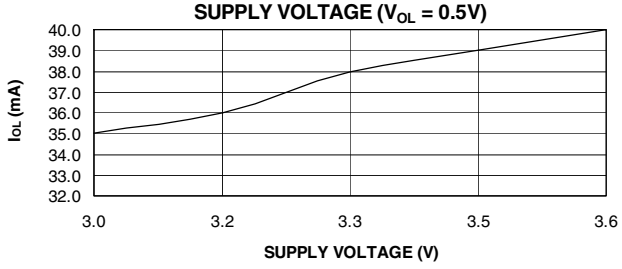
ATF22LV10CZ/CQZ SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)



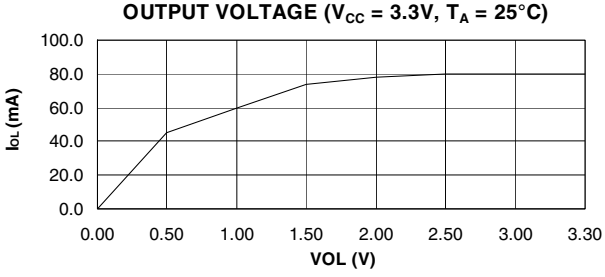
ATF22LV10C/CZ OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



ATF22LV10CZ/CQZ OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)



ATF22LV10CZ/CQZ OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



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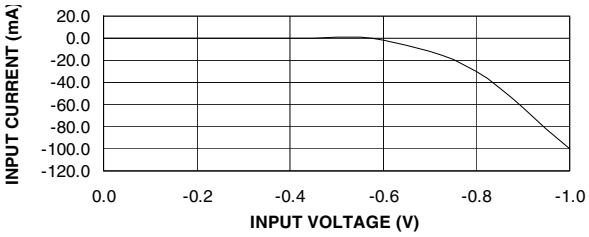
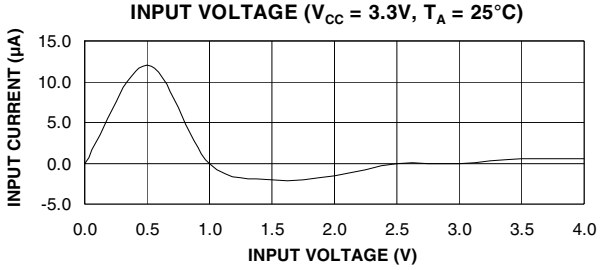
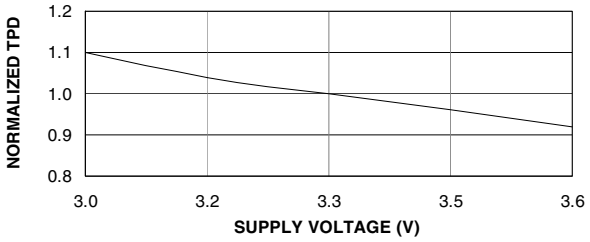
ATF22LV10CZ/CQZ INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



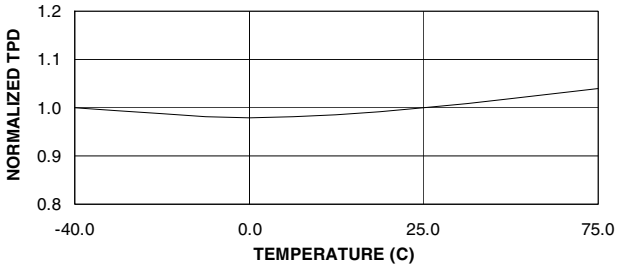
ATF22LV10CZ/CQZ INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



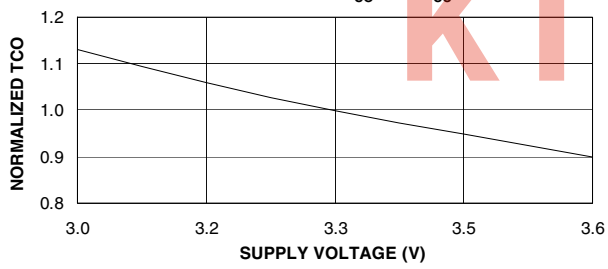
NORMALIZED T_{PD} VS. V_{CC}



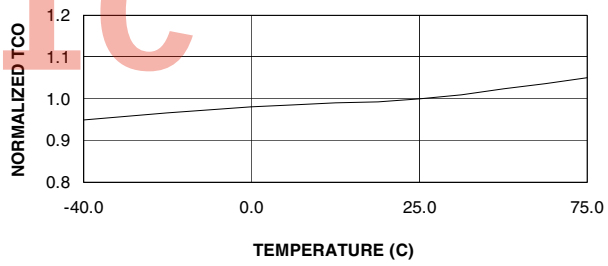
NORMALIZED T_{PD} VS. TEMP



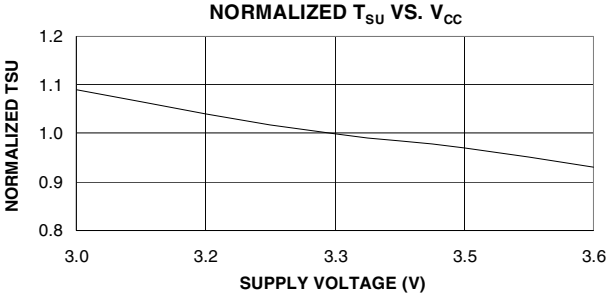
NORMALIZED T_{CO} VS. V_{CC}



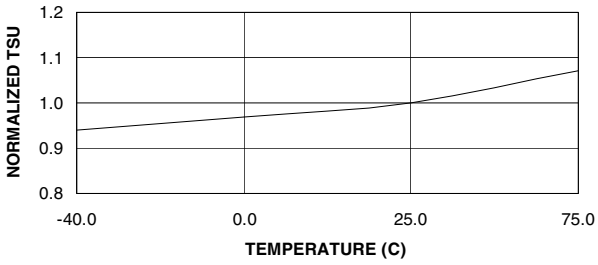
NORMALIZED T_{CO} VS. TEMP



NORMALIZED T_{SU} VS. V_{CC}



NORMALIZED T_{SU} VS. TEMP



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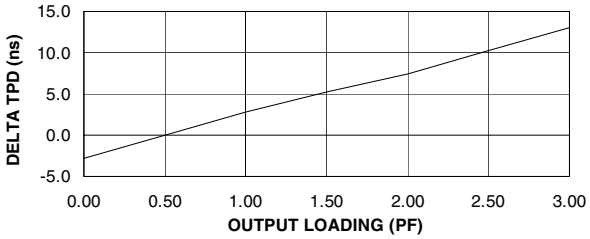
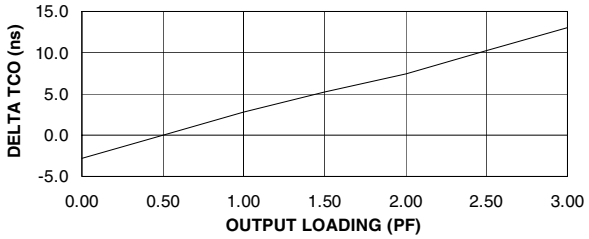
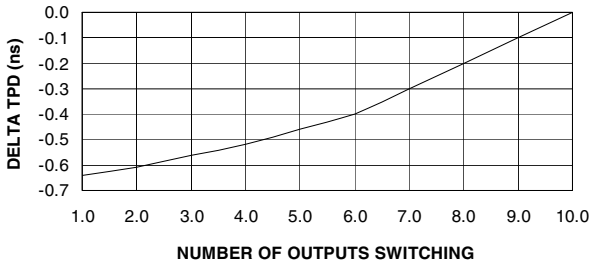
22LV10CZ/CQZ DELTA T_{PD} VS. OUTPUT LOADING



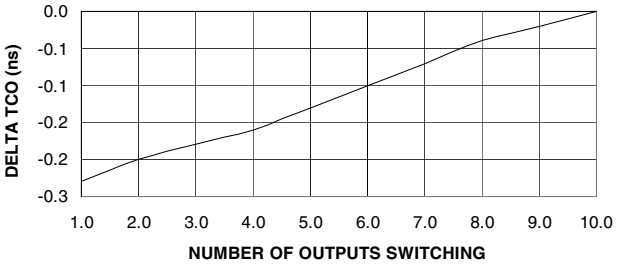
22LV10CZ/CQZ DELTA T_{CO} VS. OUTPUT LOADING



DELTA T_{PD} VS. # OF OUTPUT SWITCHING



DELTA T_{CO} VS. # OF OUTPUT SWITCHING



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10. Ordering Information

10.1 Standard Package Options

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	15	15	ATF22LV10CZ-25JC ATF22LV10CZ-25PC ATF22LV10CZ-25SC ATF22LV10CZ-25XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
			ATF22LV10CZ-25JI ATF22LV10CZ-25PI ATF22LV10CZ-25SI ATF22LV10CZ-25XI	28J 24P3 24S 24X	Industrial (-40°C to +85°C)
			ATF22LV10CQZ-30JC ATF22LV10CQZ-30PC ATF22LV10CQZ-30SC ATF22LV10CQZ-30XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
			ATF22LV10CQZ-30JI ATF22LV10CQZ-30PI ATF22LV10CQZ-30SI ATF22LV10CQZ-30XI	28J 24P3 24S 24X	Industrial (-40°C to +85°C)

10.2 ATF22LV10CQZ Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operating Range
30	15	15	ATF22LV10CQZ-30JU ATF22LV10CQZ-30PU ATF22LV10CQZ-30SU ATF22LV10CQZ-30XU	28J 24P3 24S 24X	Industrial (-40°C to +85°C)

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10.3 Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, simply de-rate I_{CC} by 15% on the “C” device. No speed de-rating is necessary.

Package Type	
28J	28-lead, Plastic J-leaded Chip Carrier (PLCC)
24P3	24-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
24X	24-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

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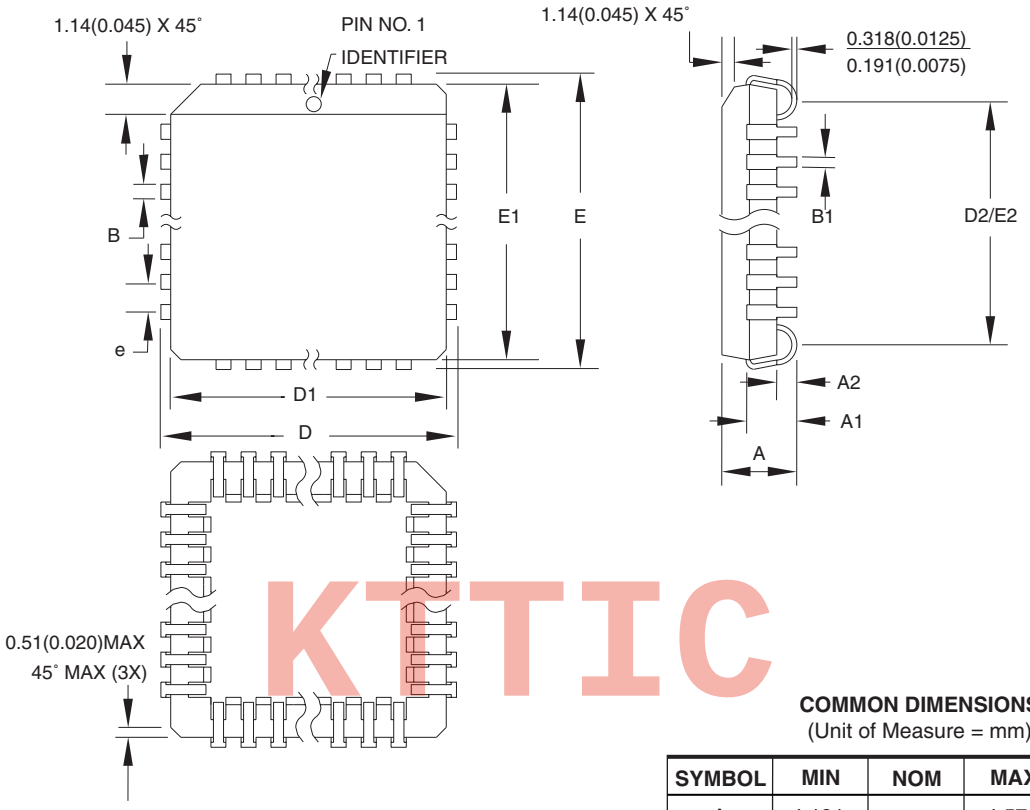
11. Packaging Information

11.1 28J – PLCC



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COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	12.319	–	12.573	
D1	11.430	–	11.582	Note 2
E	12.319	–	12.573	
E1	11.430	–	11.582	Note 2
D2/E2	9.906	–	10.922	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28J**, 28-lead, Plastic J-leaded Chip Carrier (PLCC)	28J	B

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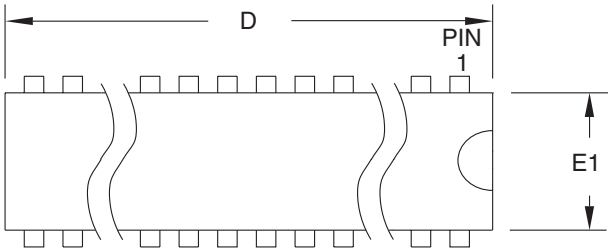
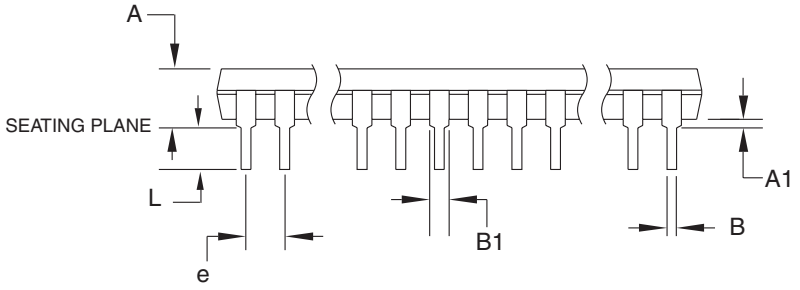
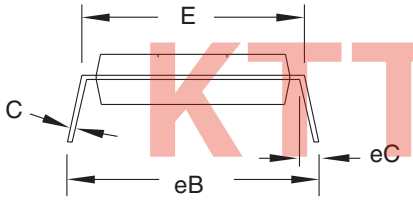
11.2 24P3 – PDIP







COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	31.623	–	32.131	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.651	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-001, Variation AF.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

6/1/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**24P3**, 24-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	24P3	D

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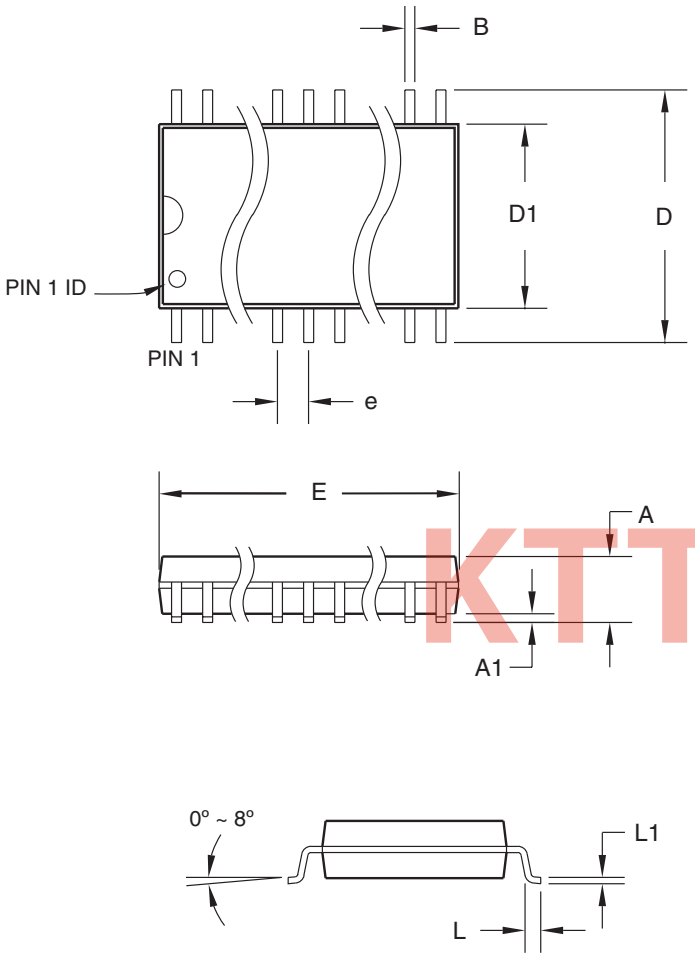
11.3 24S – SOIC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	2.65	
A1	0.10	–	0.30	
D	10.00	–	10.65	
D1	7.40	–	7.60	
E	15.20	–	15.60	
B	0.33	–	0.51	
L	0.40	–	1.27	
L1	0.23	–	0.32	
e	1.27 BSC			

06/17/2002

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**24S**, 24-lead (0.300" body) Plastic Gull Wing Small Outline (SOIC)	24S	B

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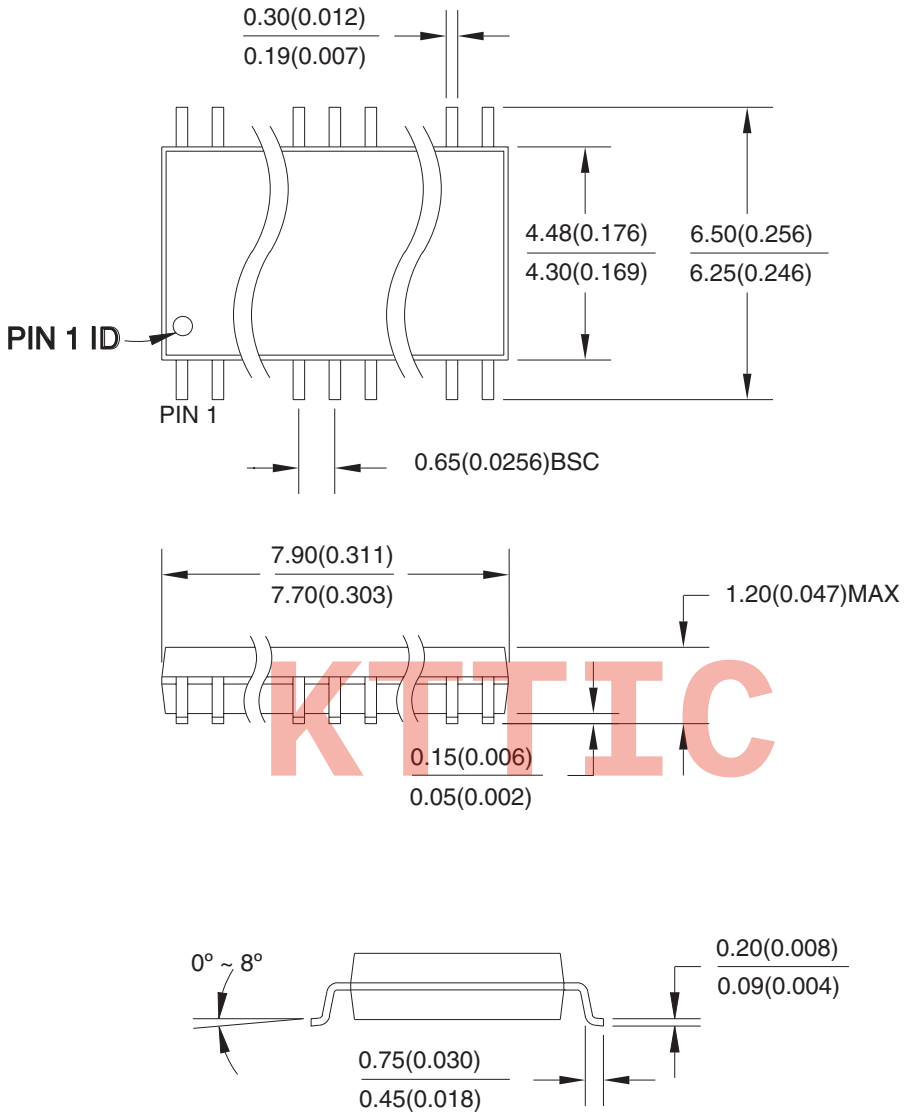
11.4 24X – TSSOP

Dimensions in Millimeter and (Inches)*
JEDEC STANDARD MO-153 AD
Controlling dimension: millimeters



04/11/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**24X**, 24-lead (4.4 mm body width) Plastic Thin Shrink Small Outline Package (TSSOP)	24X	A

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12. Revision History

Version No./Release Date	History
Revision L – November 2005	1. Added Green Package options

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