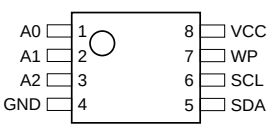
Features

- Permanent and Reversible Software Write Protection for the First-half of the Array
  - Software Procedure to Verify Write Protect Status
- Hardware Write Protection for the Entire Array
- Low-voltage and Standard-voltage Operation
  - 1.7 (V_{CC} = 1.7V to 5.5V)
- Internally Organized 256 x 8
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 100 kHz (1.7V) and 400 kHz (2.7V and 5.0V) Compatibility
- 16-byte Page Write Modes
- Partial Page Writes Are Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- 8-lead JEDEC SOIC, 8-lead Ultra Thin Mini-MAP (MLP 2x3), 8-lead TSSOP, and 8-ball dBGA2 Packages
- Die Sales: Wafer Form, Tape and Reel, and Bumped Wafers

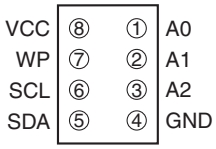
Description

The AT34C02C provides 2048 bits of serial electrically-erasable and programmable read only memory (EEPROM) organized as 256 words of 8 bits each. The first-half of the device incorporates a permanent and a reversible software write protection feature while hardware write protection for the entire array is available via an external pin. Once the permanent software write protection is enabled, by sending a special command to the device, it cannot be reversed. However, the reversible software write protection is enabled and can be reversed by sending a special command. The hardware write protection is controlled with the WP pin and can be used to protect the entire array, whether or not the software write protection has been enabled. This allows the user to protect none, first-half, or all of the array depending on the application. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT34C02C is available in space saving 8-lead JEDEC SOIC, 8-lead Ultra Thin Mini-MAP (MLP 2x3), 8-lead TSSOP, and 8-ball dBGA2 packages and is accessed via a Two-wire serial interface. It is available in 1.7V (1.7V to 5.5V).

8-lead TSSOP

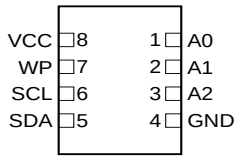


8-ball dBGA2



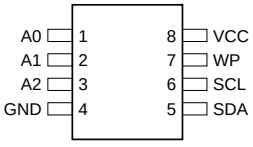
Bottom View

8-lead Ultra Thin Mini-MAP



(MLP 2x3) Bottom View

8-lead SOIC



Two-wire Serial EEPROM with Permanent and Reversible Software Write Protect

2K (256 x 8)

AT34C02C

Rev. 5185D–SEEPR–1/08

Table 0-1. Pin Configurations

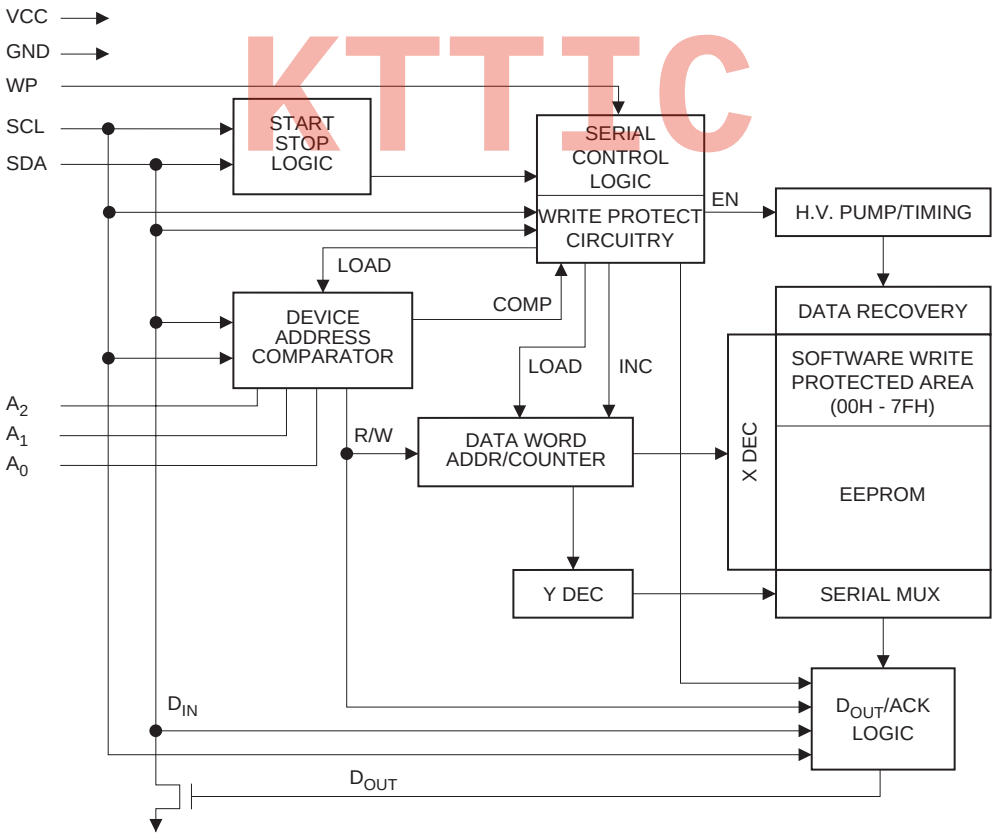
Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

1. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1-1. Block Diagram



2. Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1, and A0 pins are device address inputs that are hardwired (directly to GND or to Vcc) for compatibility with other AT24Cxx devices. When the pins are hardwired, as many as eight 2K devices may be addressed on a single bus system. (Device addressing is discussed in detail under “Device Addressing,” page 9.) A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A2, A1, and A0 pins will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the address pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

WRITE PROTECT (WP): The write protect input, when connected to GND, allows normal write operations. When WP is connected directly to Vcc, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the WP pins to a known state. When using a pull-up resistor, Atmel recommends using 10kΩ or less.

Table 2-1. AT34C02C Write Protection Modes

WP Pin Status	Permanent Write Protect Register	Reversible Write Protect Register	Part of the Array Write Protected
V_{CC}	–	–	Full Array (2K)
GND or Floating	Not Programmed	Not Programmed	Normal Read/Write
GND or Floating	Programmed	–	First-Half of Array (1K: 00H - 7FH)
GND or Floating	–	Programmed	First-Half of Array (1K: 00H - 7FH)

Table 2-2. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 100 kHz, V_{CC} = +1.7V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 2-3. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.7V to +5.5V, (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 3.6V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB3}	Standby Current V_{CC} = 5.5V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level(1)		–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level(1)		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.7V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 2-4. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to +85°C, V_{CC} = +1.7V to +5.5V, C_L = 1 TTL Gate and 100 pF (unless otherwise noted)

		1.7V		2.7V, 5.0V		
Symbol	Parameter	Min	Max	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Set-up Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time(1)		1.0		0.3	µs
t_F	Inputs Fall Time(1)		300		300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7		0.6		µs

Table 2-4. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to +85°C, V_{CC} = +1.7V to +5.5V, C_L = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	1.7V		2.7V, 5.0V		Units
		Min	Max	Min	Max	
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance[1]	25°C, Page Mode	1M		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

3. Memory Organization

AT34C02C, 2K Serial EEPROM: The 2K is internally organized with 16 pages of 16 bytes each. Random word addressing requires a 8-bit data word address.

4. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 4-3 on page 7). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 4-4 on page 7).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 4-4 on page 7).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT34C02C features a low-power standby mode which is enabled: (a) upon power-up or (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any Two-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition.

Figure 4-1. Bus Timing SCL: Serial Clock SDA: Serial Data I/O

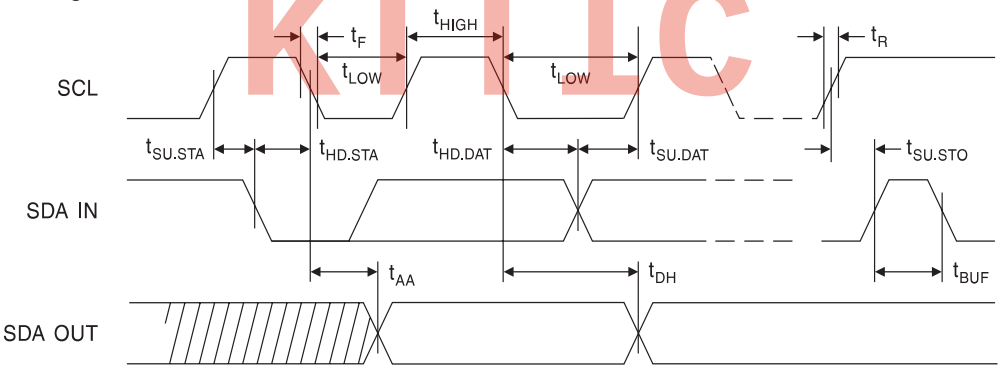
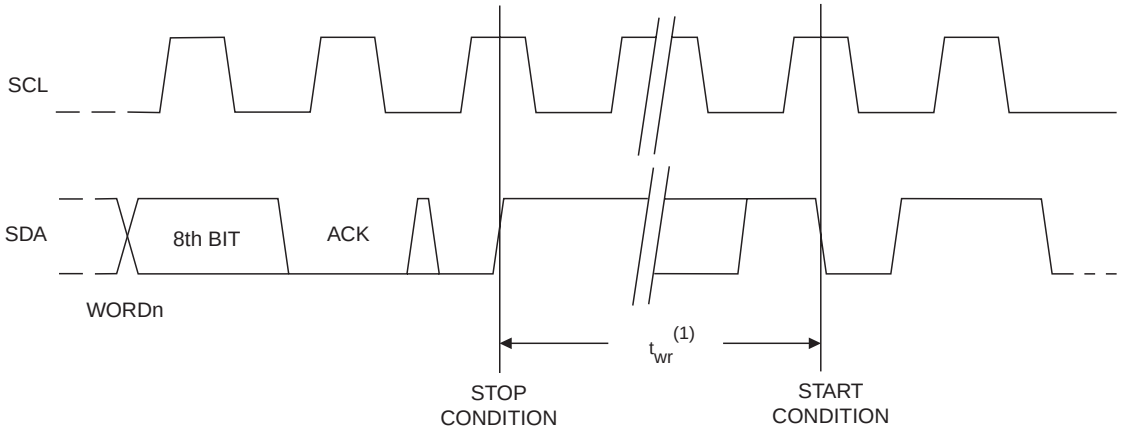


Figure 4-2. Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 4-3. Data Validity

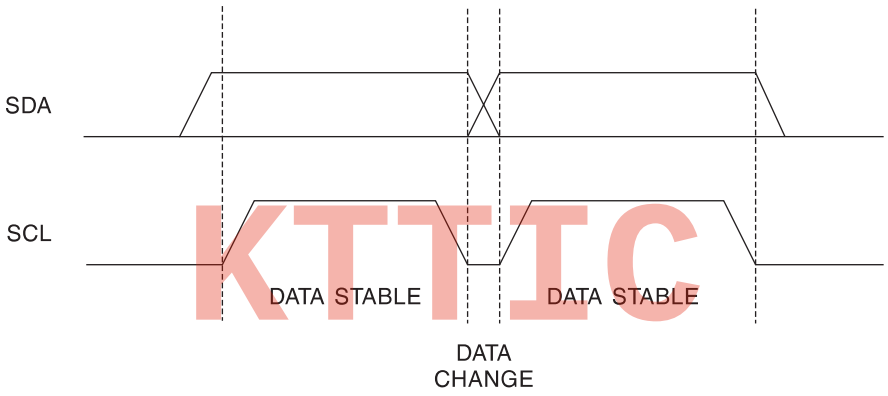


Figure 4-4. Start and Stop Condition

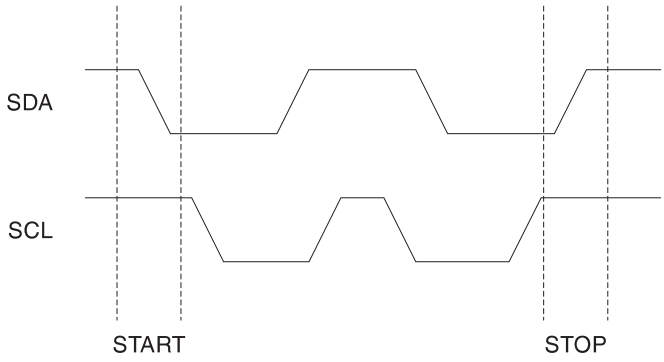
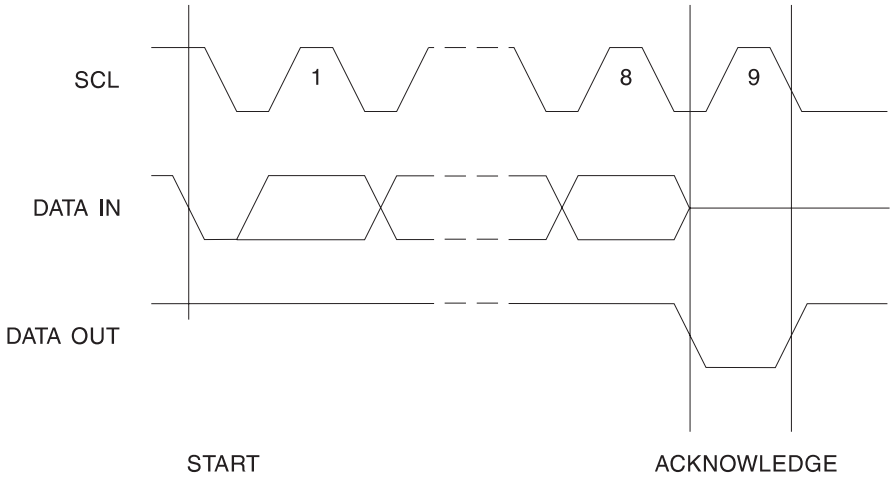


Figure 4-5. Output Acknowledge



5. Device Addressing

The 2K EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 8-1 on page 13).

The device address word consists of a mandatory one-zero sequence for the first four most-significant bits (1010) for normal read and write operations and 0110 for writing to the write protect register.

The next 3 bits are the A2, A1 and A0 device address bits for the AT34C02C EEPROM. These 3 bits must compare to their corresponding hard-wired input pins.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state. The device will not acknowledge if the write protect register has been programmed and the control code is 0110.

6. Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8-2 on page 13).

The device will acknowledge a write command, but not write the data, if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

PAGE WRITE: The 2K device is capable of 16-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 1 on page 13).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

The device will acknowledge a write command, but not write the data, if the software or hardware write protection has been enabled. The write cycle time must be observed even when the write protection is enabled.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

7. Write Protection

The software write protection, once enabled, write protects only the first-half of the array (00H - 7FH) while the hardware write protection, via the WP pin, is used to protect the entire array.

PERMANENT SOFTWARE WRITE PROTECTION: The software write protection is enabled by sending a command, similar to a normal write command, to the device which programs the permanent write protect register. This must be done with the WP pin low. The write protect register is programmed by sending a write command with the device address of 0110 instead of 1010 with the address and data bit being don’t cares (see Figure 7-1 on page 10). Once the software write protection has been enabled, the device will no longer acknowledge the 0110 control byte. The software write protection cannot be reversed even if the device is powered down. The write cycle time must be observed.

REVERSIBLE SOFTWARE WRITE PROTECTION: The reversible software write protection is enabled by sending a command, similar to a normal write command, to the device which programs the reversible write protect register. This must be done with the WP pin low. The write protect register is programmed by sending a write command 01100010 with pins A2 and A1 tied to ground or don't connect and pin A0 connected to VHV (see Figure 7-2). The reversible write protection can be reversed by sending a command 01100110 with pin A2 tied to ground or no connect, pin A1 tied to VCC and pin A0 tied to VHV (see Figure 7-3).

HARDWARE WRITE PROTECTION: The WP pin can be connected to V_{CC}, GND, or left floating. Connecting the WP pin to V_{CC} will write protect the entire array, regardless of whether or not the software write protection has been enabled. The software write protection register cannot be programmed when the WP pin is connected to V_{CC}. If the WP pin is connected to GND or left floating, the write protection mode is determined by the status of the software write protect register.

Figure 7-1. Setting Permanent Write Protect Register (PSWP)

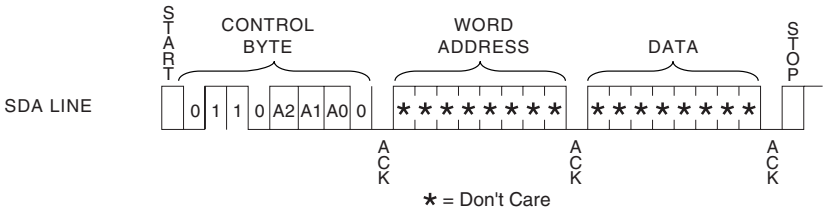


Figure 7-2. Setting Reversible Write Protect Register (RSWP)

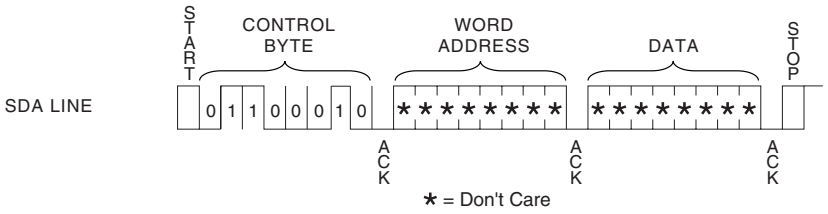


Figure 7-3. Clearing Reversible Write Protect Register (RSWP)

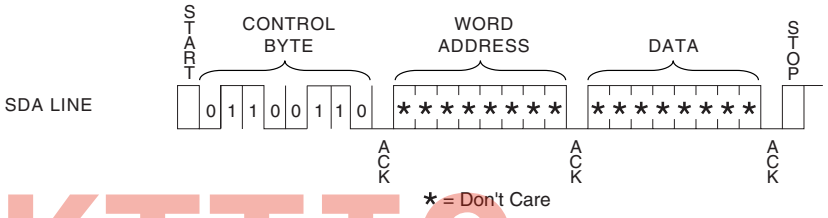


Table 7-1. Write Protection

	Pin			Preamble							RW
Command	**A2**	**A1**	**A0**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Set PSWP	A2	A1	A0	0	1	1	0	A2	A1	A0	0
Set RSWP	0	0	VHV	0	1	1	0	0	0	1	0
Clear RSWP	0	1	VHV	0	1	1	0	0	1	1	0

Table 7-2. VHV

	Min	Max	Units
VHV	7	10	V

Note: VHV - VCC > 4.8V

Table 7-3. WP Connected to GND or Floating

WP Connected to GND or Floating					
Command	**R/W Bit**	**Permanent Write Protect Register PSWP**	**Reversible Write Protect Register RSWP**	**Acknowledgment from Device**	**Action from Device**
1010	R	X	X	ACK	
1010	W	Programmed	X	ACK	Can write to second Half (80H - FFH) only
1010	W	X	Programmed	ACK	Can write to second Half (80H - FFH) only
1010	W	Not Programmed	Not Programmed	ACK	Can write to full array
Read PSWP	R	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Read PSWP	R	Not Programmed	X	ACK	Read out data don't care. Indicates PSWP register is not programmed
Set PSWP	W	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Set PSWP	W	Not Programmed	X	ACK	Program permanent write protect register (irreversible)
Read RSWP	R	X	Programmed	No ACK	STOP - Indicates reversible write protect register is programmed
Read RSWP	R	X	Not Programmed	ACK	Read out data don't care. Indicates RSWP register is not programmed
Set RSWP	W	X	Programmed	No ACK	STOP - Indicates reversible write protect register is programmed
Set RSWP	W	X	Not Programmed	ACK	Program reversible write protect register (reversible)
Clear RSWP	W	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Clear RSWP	W	Not Programmed	X	ACK	Clear (unprogram) reversible write protect register (reversible)

Table 7-4. WP Connected to Vcc

WP Connected to Vcc					
Command	**R/W Bit**	**Permanent Write Protect Register PSWP**	**Reversible Write Protect Register RSWP**	**Acknowledgment from Device**	**Action from Device**
1010	R	X	X	ACK	Read array
1010	W	X	X	ACK	Device Write Protect
Read PSWP	R	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Read PSWP	R	Not Programmed	X	ACK	Read out data don't care. Indicates PSWP register is not programmed

WP Connected to Vcc					
Set PSWP	W	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Set PSWP	W	Not Programmed	X	ACK	Cannot program write protect registers
Read RSWP	R	X	Programmed	No ACK	STOP - Indicates reversible write protect register is programmed
Read RSWP	R	X	Not Programmed	ACK	Read out data don't care. Indicates RSWP register is not programmed
Set RSWP	W	X	Programmed	No ACK	STOP - Indicates reversible write protect register is programmed
Set RSWP	W	X	Not Programmed	ACK	Cannot program write protect registers
Clear RSWP	W	Programmed	X	No ACK	STOP - Indicates permanent write protect register is programmed
Clear RSWP	W	Not Programmed	X	ACK	Cannot write to write protect registers

8. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. To end the command, the microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 8-3 on page 14).

RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. To end the command, the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 8-4 on page 14).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 8-5 on page 14).

PERMANENT WRITE PROTECT REGISTER (PSWP) STATUS: To find out if the register has been programmed, the same procedure is used as to program the register except that the R/W bit is set to 1. If the device sends an acknowledge, then the permanent write protect register has not been programmed. Otherwise, it has been programmed and the device is permanently write protected at the first half of the array.

Table 8-1. PSWP Status

	Pin			Preamble							RW
Command	**A2**	**A1**	**A0**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Read PSWP	A2	A1	A0	0	1	1	0	A2	A1	A0	1

REVERSIBLE WRITE PROTECT REGISTER(RSWP) STATUS: To find out if the register has been programmed, the same procedure is used as to program the register except that the R/W bit is set to 1. If the sends an device acknowledge, then the reversible write protect register has not been programmed. Otherwise, it has been programmed and the device is write protected (reversible) at the first half of the array.

Figure 8-1. Device Address

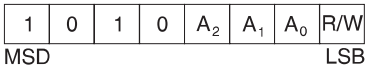


Figure 8-2. Byte Write

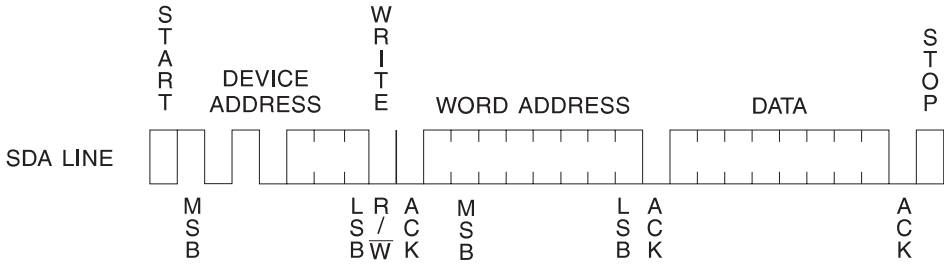


Figure 1. Page Write

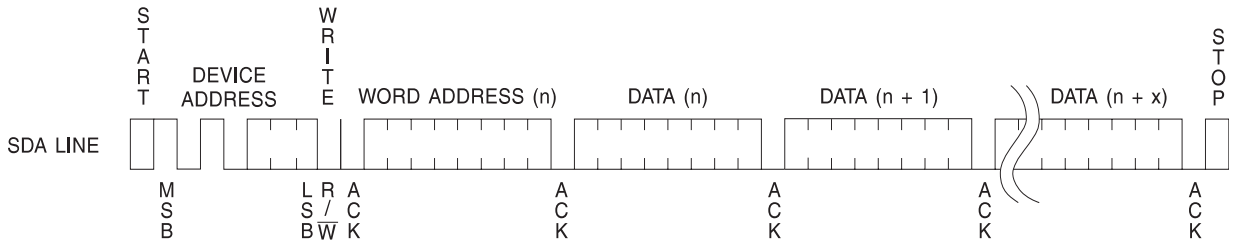


Figure 8-3. Current Address Read

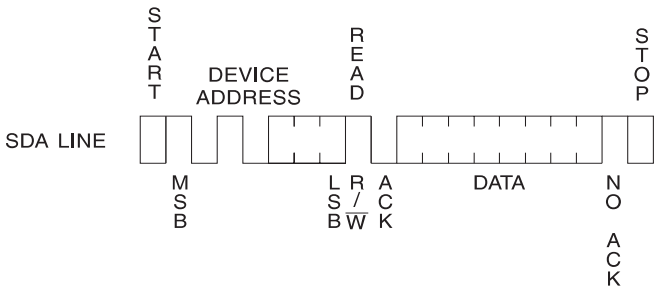


Figure 8-4. Random Read

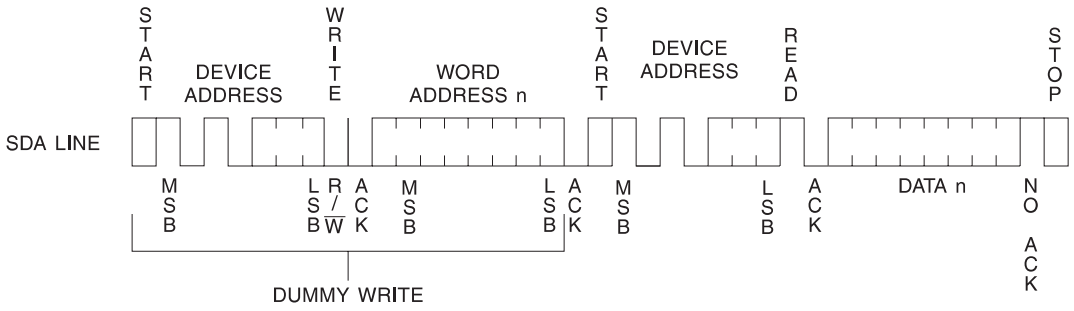
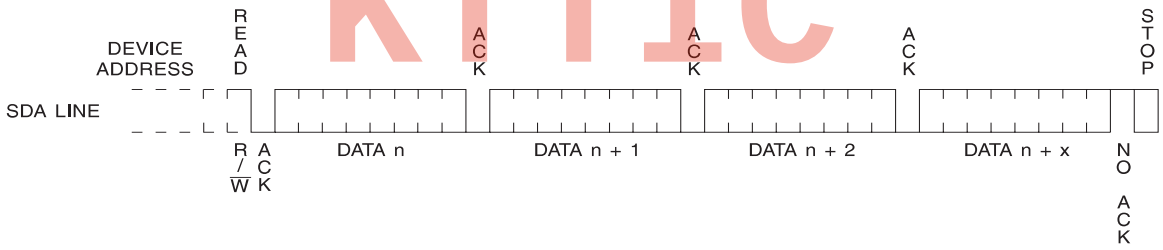


Figure 8-5. Sequential Read



AT34C02C Ordering Information

Ordering Code	Package	Operation Range
AT34C02CN-SH-B[1] (NiPdAu Lead Finish)	8S1	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT34C02CN-SH-T[2](NiPdAu Lead Finish)	8S1	
AT34C02C-TH-B[1] (NiPdAu Lead Finish)	8A2	
AT34C02C-TH-T[2] (NiPdAu Lead Finish)	8A2	
AT34C02CY6-YH-T[2](NiPdAu Lead Finish)	8Y6	
AT34C02CU3-UU-T[2]	8U3-1	

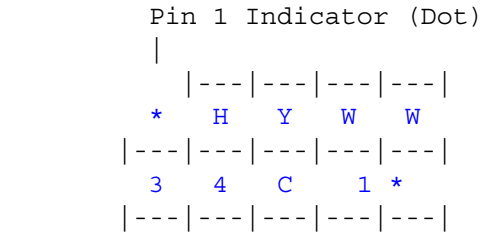
Notes: 1. “-B” denotes bulk.
2. “-T” denotes tape and reel. SOIC = 4K per reel; TSSOP, Ultra Thin Mini MAP and dBGA2 = 5K per reel.

Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead Package (DFN), (MLP 2x3 mm)
8U3-1	8-ball, die Ball Grid Array Package (dBGA2)
Options	
–1.7	Low Voltage (1.7V to 5.5V)

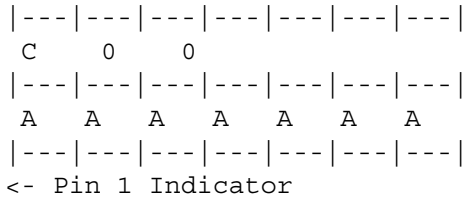
9. New part marking

9.3 8-TSSOP

TOP MARK



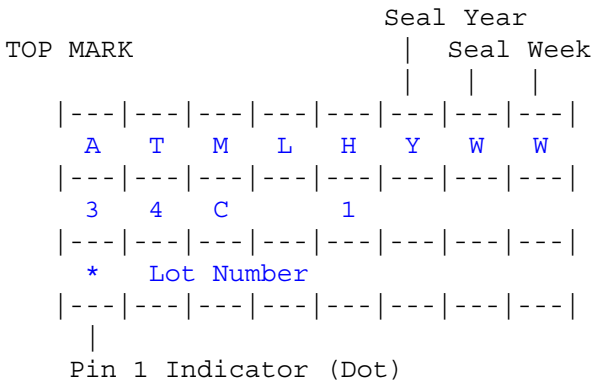
BOTTOM MARK



Country of Origin
Atmel Lot #

Y = SEAL YEAR		WW = SEAL WEEK
6: 2006	0: 2010	02 = Week 2
7: 2007	1: 2011	04 = Week 4
8: 2008	2: 2012	:: : :::: :
9: 2009	3: 2013	:: : :::: ::
		50 = Week 50
		52 = Week 52

9.4 8-SOIC



Y = SEAL YEAR

6: 2006
7: 2007
8: 2008
9: 2009
0: 2010
1: 2011
2: 2012
3: 2013

WW = SEAL WEEK

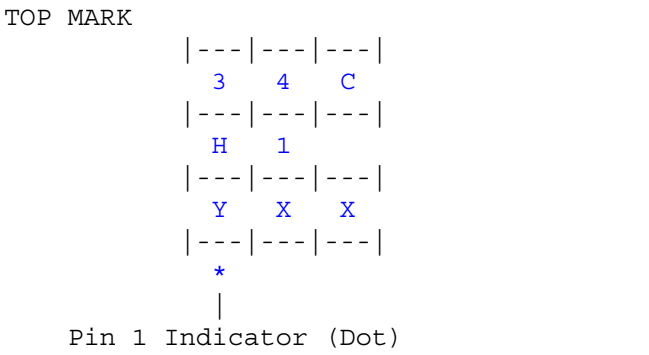
02 = Week 2
04 = Week 4
:: : :::: :
:: : :::: ::
50 = Week 50
52 = Week 52

Lot Number to Use ALL Characters in Marking

BOTTOM MARK

No Bottom Mark

9.5 8-Ultra Thin Mini MAP



Y = YEAR OF ASSEMBLY

XX = ATMEL LOT NUMBER TO COORESPOND WITH NSEB TRACE CODE LOG BOOK.
(e.g. XX = AA, AB, AC,...AX, AY, AZ)

Y = SEAL YEAR

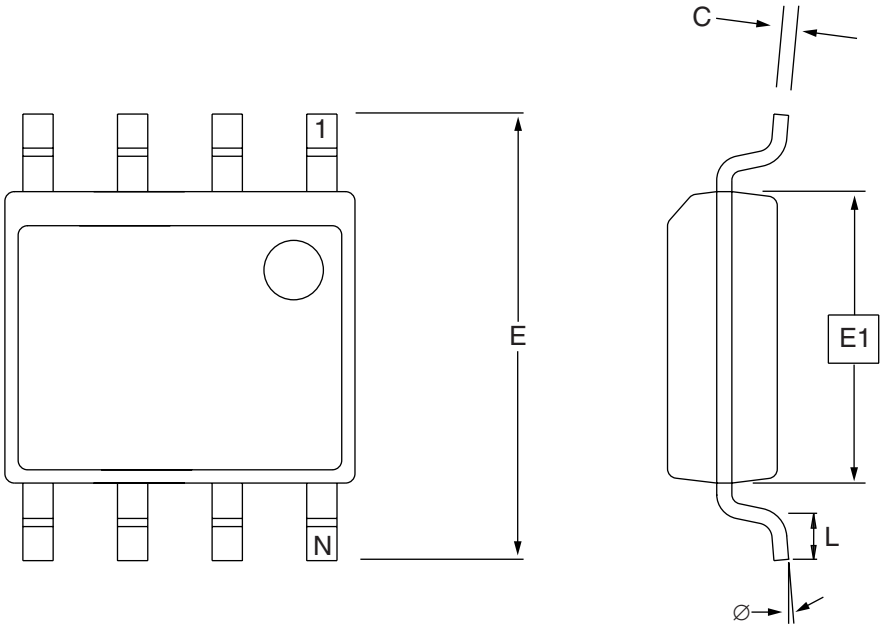
6: 2006	0: 2010
7: 2007	1: 2011
8: 2008	2: 2012
9: 2009	3: 2013

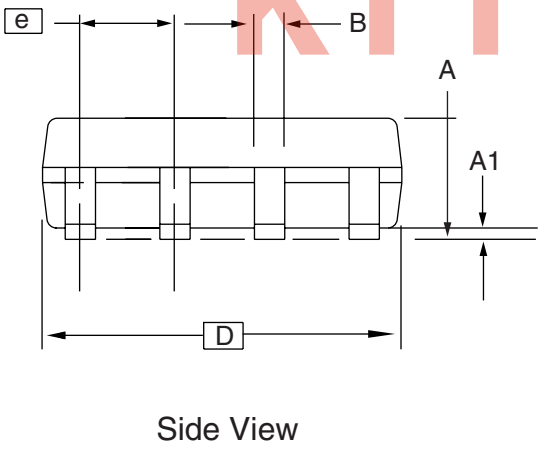
9.6 dBGA2

```
TOP MARK

LINE 1------->    34CU
LINE 2------->    YMTC
                  |<--  Pin 1 This Corner


 Y = ONE DIGIT YEAR CODE
4: 2004   7: 2007
5: 2005   8: 2008
6: 2006   9: 2009

M = SEAL MONTH (USE ALPHA DESIGNATOR A-L)
A = JANUARY
 B = FEBRUARY
" " """""""
J = OCTOBER
 K = NOVEMBER
 L = DECEMBER


    TC = TRACE CODE (ATMEL LOT
    NUMBERS TO CORRESPOND
    WITH ATK TRACE CODE LOG BOOK)
```

10. Packaging Information

8S1 – JEDEC SOIC





COMMON DIMENSIONS
(Unit of Measure = mm)

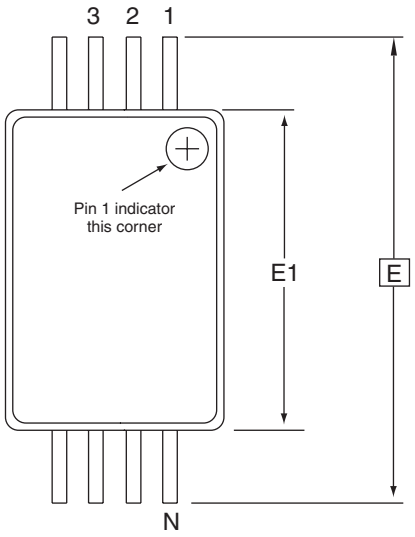
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

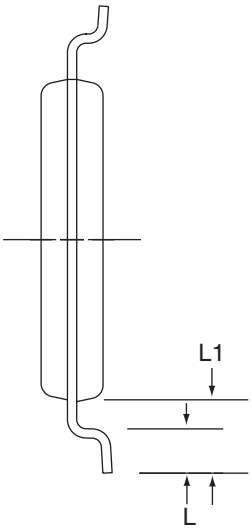
10/7/03

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** B

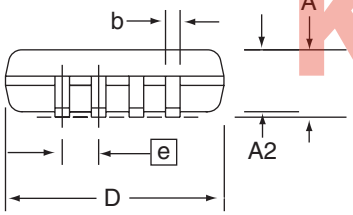
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

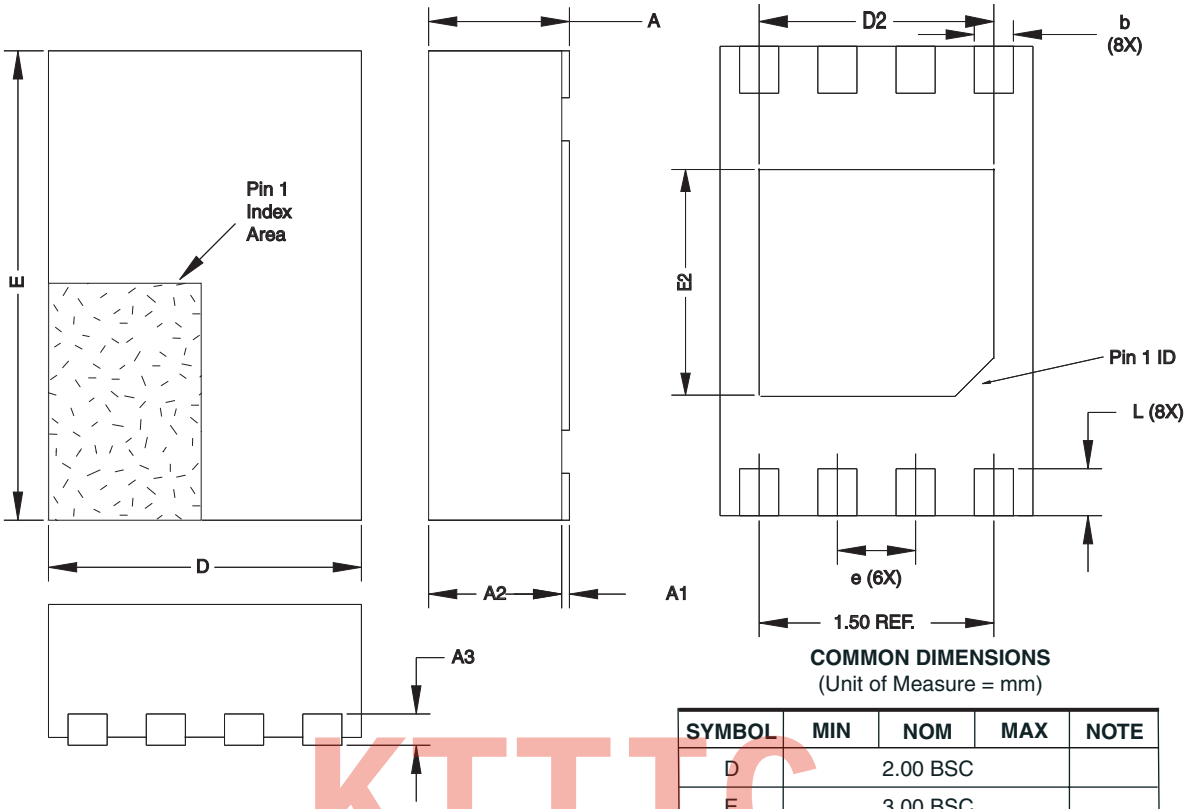
SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	8A2	B

8Y6 – Mini-MAP



COMMON DIMENSIONS
(Unit of Measure = mm)

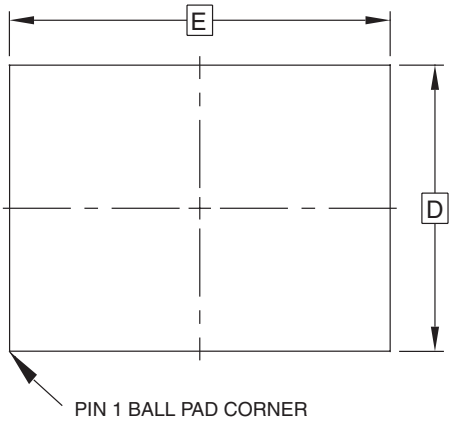
SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	-	-	1.40	
A	-	-	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
A3		0.20 REF		
L	0.20	0.30	0.40	
e		0.50 BSC		
b	0.20	0.25	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

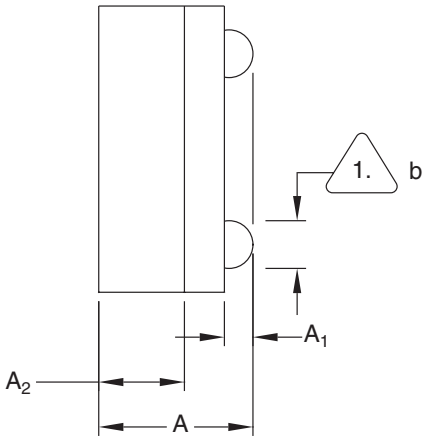
10/16/07

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8Y6**, 8-lead 2.0 x 3.0 mm Body, 0.50 mm Pitch, Utlra Thin Mini-Map, Dual No Lead Package (DFN) ,(MLP 2x3)	8Y6	D

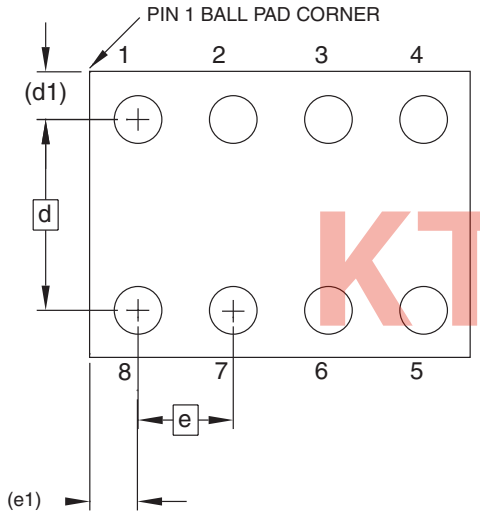
8U3-1 – dBGA2



Top View



Side View



Bottom View
8 SOLDER BALLS

1. This drawing is for general information only.
2. Dimension 'b' is measured at maximum solder ball diameter

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.71	0.81	0.91	
A1	0.10	0.15	0.20	
A2	0.40	0.45	0.50	
b	0.20	0.25	0.30	2
D	1.50 BSC			
E	2.00 BSC			
e	0.50 BSC			
e1	0.25 REF			
d	1.00 BSC			
d1	0.25 REF			

6/24/03

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8U3-1,** 8-ball, 1.50 x 2.00 mm Body, 0.50 mm pitch, Small Die Ball Grid Array Package (dBGA2)	PO8U3-1	A

11. Revision History

Doc. Rev.	Date	Comments
5185D	1/2008	Removed ‘preliminary’ status
5185C	8/2007	Updated to new template Added Package Marking tables
5185B	3/2007	Implemented revision history