Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
  - Datasheet describes Mode 0 Operation
- 50 MHz Clock Rate
- Byte Mode and Page Mode Program (1 to 256 Bytes) Operations
- Sector/Block/Page Architecture
  - 256 byte Pages per Sector
  - Eight 4 Kbyte Sectors per Block
  - Four uniform 32 Kbyte Blocks
- Self-timed Sector, Block and Chip Erase
- Product Identification Mode with JEDEC Standard
- Low-voltage Operation
  - 2.7V (V_{CC} = 2.7V to 3.6V)
- Hardware and Software Write Protection
  - Device protection with Write Protect ($\overline{WP}$) Pin
  - Write Enable and Write Disable Instructions
  - Software Write Protection:
    - Upper 1/32, 1/16, 1/8, 1/4, 1/2 or Entire Array
- Flexible Op Codes for Maximum Compatibility
- Self-timed Program Cycle
  - 30 µs/Byte Typical
- Single Cycle Reprogramming (Erase and Program) for Status Register
- High Reliability
  - Endurance: 10,000 Write Cycles Typical
- 8-lead JEDEC 150mil SOIC and 8-lead Ultra Thin Small Array Package (SAP)
- Die Sales: Waffer Form, Tape and Reel, and Bumped Waffers

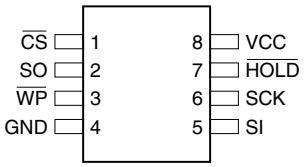
Description

The AT25FS010 provides 1,048,576 bits of serial reprogrammable Flash memory organized as 131,072 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT25FS010 is available in a space-saving 8-lead JEDEC SOIC and 8-lead Ultra Thin SAP packages.

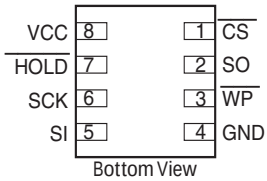
Table 0-1. Pin Configuration

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

8-lead JEDEC SOIC



8-lead SAP



High Speed Small Sectored SPI Flash Memory

1M (131,072 x 8)

AT25FS010

5167D–SFLSH–8/07

The AT25FS010 is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All write cycles are completely self-timed.

BLOCK WRITE protection for upper 1/32, 1/16, 1/8, 1/4, 1/2 or the entire memory array is enabled by programming the status register. Separate write enable and write disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

1. Absolute Maximum Ratings*

Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +5.0V
Maximum Operating Voltage	4.2V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1-1. Block Diagram

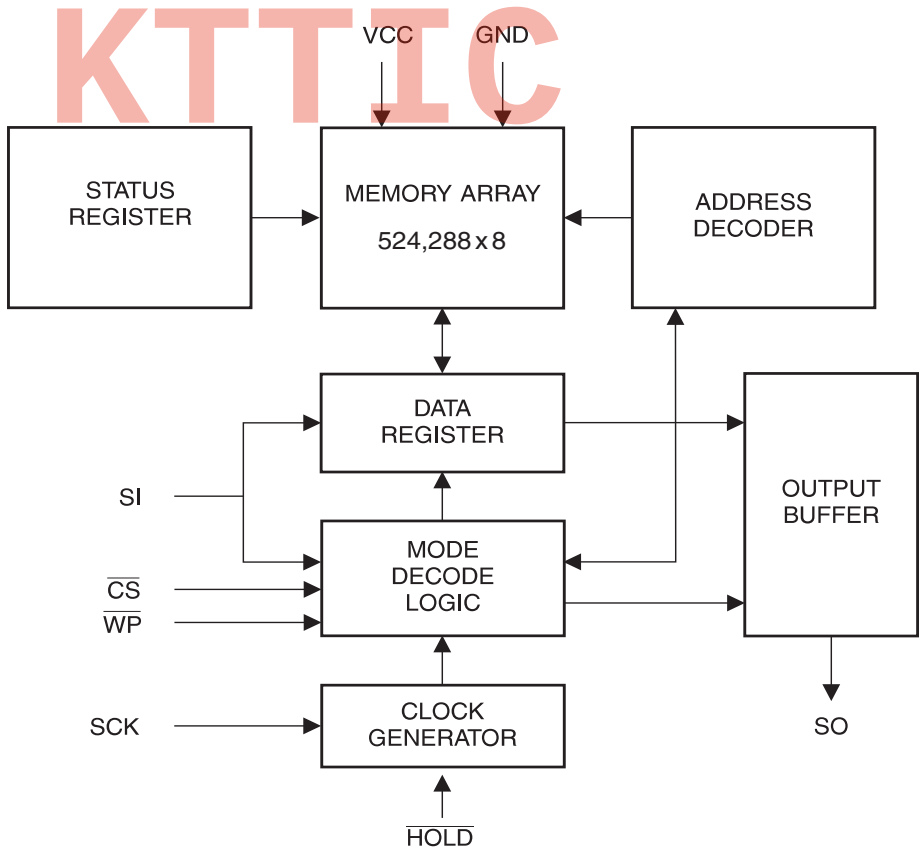


Table 1-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +3.6V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 1-2. DC Characteristics (Preliminary – Subject to Change)

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +2.7V to +3.6V, T_{AC} = 0°C to +70°C, V_{CC} = +2.7V to +3.6V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC}	Supply Voltage			2.7		3.6	V
I_{CC1}	Supply Current	V_{CC} = 3.6V at 20 MHz, SO = Open Read			10.0	17.0	mA
I_{CC2}	Supply Current	V_{CC} = 3.6V at 20 MHz, SO = Open Write			15.0	45.0	mA
I_{SB}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}			2.0	10.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		-3.0		3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		-3.0		3.0	µA
V_{IL}[1]	Input Low Voltage			-0.6		V_{CC} x 0.3	V
V_{IH}[1]	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA			0.2	V
V_{OH}	Output High Voltage		I_{OH} = -100 µA	V_{CC} - 0.2			V

Note: 1. V_{IL} and V_{IH} max are reference only and are not tested.

Table 1-3. AC Characteristics (Preliminary – Subject to Change)

Applicable over recommended operating range from T_A = –40°C to +85°C, V_{CC} = +2.7V to +3.6V
C_L = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Clock Frequency	0		50	MHz
t_{RI}	Input Rise Time			5	ns
t_{FI}	Input Fall Time			5	ns
t_{WH}	SCK High Time	9			ns
t_{WL}	SCK Low Time	9			ns
t_{CS}	$\overline{CS}$ High Time	100			ns
t_{CSS}	$\overline{CS}$ Setup Time	5			ns
t_{CSH}	$\overline{CS}$ Hold Time	5			ns
t_{SU}	Data In Setup Time	5			ns
t_H	Data In Hold Time	5			ns
t_{HD}	$\overline{Hold}$ Setup Time	5			ns
t_{CD}	$\overline{Hold}$ $\overline{Hold}$ Time	5			ns
t_V	Output Valid			9	ns
t_{HO}	Output Hold Time	0			ns
t_{LZ}	$\overline{Hold}$ to Output Low Z			9	ns
t_{HZ}	$\overline{Hold}$ to Output High Z			9	ns
t_{DIS}	Output Disable Time			9	ns
t_{se}	Sector Erase Time		50	200	ms
t_{be}	Block Erase Time		200	500	ms
t_{ce}	Chip Erase Time		1.6	4	s
t_{SR}	Status Register Write Cycle Time			60	ms
t_{BPC}	Byte Program Cycle Time(1)		30	50	µs
Endurance(2)			10K		Write Cycles(3)

Notes: 1. The programming time for n bytes will be equal to n x t_{BPC}.
2. This parameter is ensured by characterization at 3.0v, 25c only.
3. One write cycle consists of erasing a sector, followed by programming the same sector.

2. Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the Serial Clock pin (SCK) is always an input, the AT25FS010 always operates as a slave.

TRANSMITTER/RECEIVER: The AT25FS010 has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25FS010, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25FS010 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25FS010. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The AT25FS010 has a write lockout feature that can be activated by asserting the write protect pin ($\overline{WP}$). When the lockout feature is activated, locked-out sectors will be READ only. The write protect pin will allow normal read/write operations when held high. When the $\overline{WP}$ is brought low and WPEN bit is “1”, all write operations to the status register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal status register write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is “0”. This will allow the user to install the AT25FS010 in a system with the $\overline{WP}$ pin tied to ground and still be able to write to the status register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to “1”.

3. Operating Features

3.1 Recommended Power-up

When the power supply is turned on, V_{cc} rises monotonically from ground to the full operating V_{cc}. During this time, the Chip Select (CS) signal is not allowed to float and must follow V_{cc}. For this reason, it is recommended to use a suitable pull-up resistor connected between CS and V_{cc}. The device is ready for communication once a stable V_{cc} is reached within the specified operating voltage range.

3.2 Recommended Power-down

The device must be deselected and in Standby and Write Disabled mode prior to V_{cc} power down sequence. This means there should be no write operation/internal Write cycle or read operation in progress during the Chip Select (CS) line must be allowed to follow V_{cc} during power down. After power down, it is recommended V_{cc} should be held at ground level for at least 0.5 seconds before power up again.

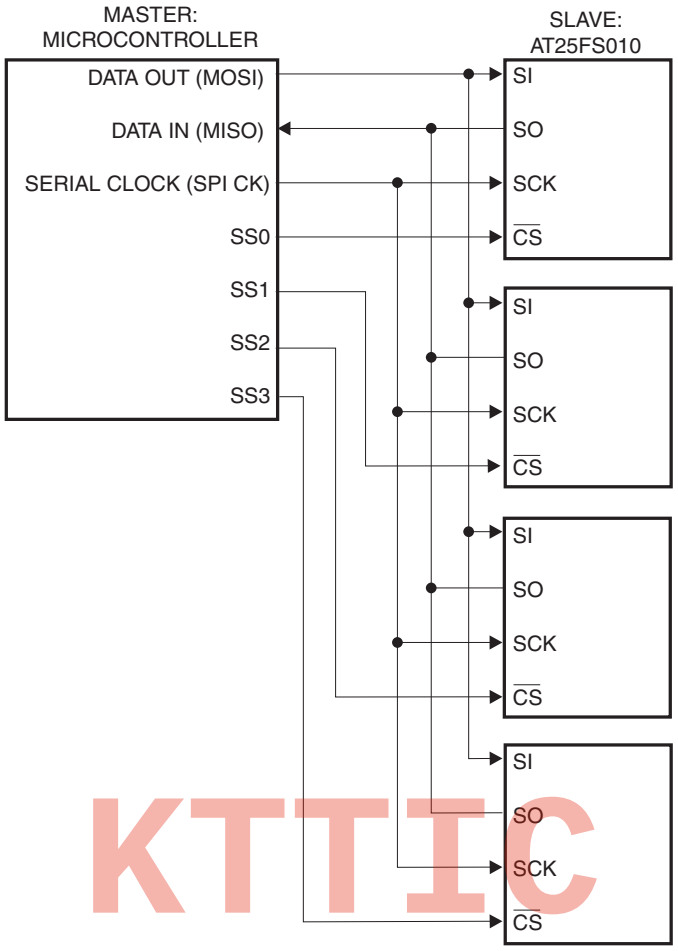
3.3 Power On Reset Protection

In order to prevent data corruption and inadvertent Write operations during device power-up and power down, a Power On Reset (POR) circuit is enabled. At Power-up (continuous rise of V_{cc} from 0v), the device will not respond to any instruction and will be held in reset (which puts the device in standby mode) until the V_{cc} has reached the Power On Reset threshold voltage. This threshold is lower than the minimum specified V_{cc} operation voltage.

At power down (continuous fall of V_{cc}), when V_{cc} drops from the operating voltage below the POR threshold, all operations are disabled and the device will not respond to any command. A stable and valid V_{cc} must be applied before executing and communication.

Please note: The POR threshold trip point is ~1.8v for Serial Flash products and is ensured by design to have a reset during power up and power down and is not 100% tested.

Figure 3-1. SPI Serial Interface



4. Functional Description

The AT25FS010 is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6800 type series of microcontrollers.

The AT25FS010 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 4-1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Write is defined as program and/or erase in this specification. The following commands, PROGRAM, SECTOR ERASE, BLOCK ERASE, CHIP ERASE, and WRSR are write instructions for AT25FS010.

Table 4-1. Instruction Set for the AT25FS010

Instruction Name	One Byte OpCode		Operation
	Binary	Hex	
WREN	0000 X110	06	Set Write Enable Latch
WRDI	0000 X100	04	Reset Write Enable Latch
RDSR	0000 X101	05	Read Status Register
WRSR	0000 X001	01	Write Status Register
READ	0000 0011	03	Read Data from Memory Array
FAST READ	0000 1011	0B	Read Data from Memory Array (with dummy cycles)
PROGRAM	0000 X010	02	Program Data Into Memory Array
SECTOR ERASE (1)	0010 0000	20	Erase One 4kbyte Sector in Memory Array
	1101 0111	D7	
BLOCK ERASE(1)	0101 0010	52	Erase One 32kbyte Block in Memory Array
	1101 1000	D8	
CHIP ERASE(1)	0110 0000	60	Erase All Memory Array
	1100 0111	C7	
RDID(1)	1001 1111	9F	Read Manufacturer and Product ID
	1010 1011	AB	

Note: 1. **Either one of the OP CODES will execute the instruction.**

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All write instructions must therefore be preceded by the WREN instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the WRDI instruction disables all write commands. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

READ STATUS REGISTER (RDSR): The RDSR instruction provides access to the status register. The READY/BUSY and write enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed.

These bits are set by using the WRSR instruction. During internal write cycles, all other commands will be ignored except the RDSR instruction.

Table 4-2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	BP4	BP3	X	BP1	BP0	WEN	$\overline{RDY}$

Note: X = Don't Care

Table 4-3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = 0 ($\overline{RDY}$) indicates the device is READY. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1 = 0 indicates the device *is not* WRITE ENABLED. Bit 1 = 1 indicates the device is WRITE ENABLED.
Bit 2 (BP0)	See Table 4-5.
Bit 3 (BP1)	See Table 4-5.
Bit 4	Not Used
Bit 5 (BP3)	See Table 4-5.
Bit 6 (BP4)	See Table 4-5.
Bit 7 (WPEN)	See Table 4-6.
Bits 0-7 are 1s during an internal write cycle.	

READ PRODUCT ID (RDID): The RDID instruction allows the user to read the manufacturer ID byte followed by two device ID bytes. The manufacturer ID is assigned by JEDEC and is 1Fh for Atmel (see Table 4-4). The first device ID byte indicates the memory type (66h=AT25FS010) followed by the device memory capacity byte (01h). For maximum compatibility and flexibility, two RDID opcodes (9Fh and ABh) are supported and will perform the same operation.

Table 4-4. Read Product ID (RDID)

Manufacturer ID	Device ID	
	Memory Type	Memory Capacity
1Fh	66h	01h

The device is first selected by driving Chip Select ($\overline{CS}$) low then the RDID opcode is shifted in on Serial In (SI) during rising edge of clock. The 24-bit Manufacturer and Device Identification Codes stored in memory are clocked out on Serial Output (SO) starting on the falling edge of clock (see Figure 5-13). If $\overline{CS}$ stays low after the last bit of second device ID byte is shifted out, the manufacturer ID and 2 byte device ID will continue to be clocked out until $\overline{CS}$ goes high. The RDID sequence is terminated any time $\overline{CS}$ is driven high and the device will go into standby mode.

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of eight levels of protection for the AT25FS010. The AT25FS010 is divided into eight blocks where the top 1/32, 1/16, 1/8, top quarter (1/4), top half (1/2), or all of the memory blocks can be protected (locked out) from write. Any of the locked-out blocks will therefore be READ only. The

locked-out sector/block and the corresponding status register control bits are shown in Table 4-5 on page 10.

The six bits, BP0, BP1, BP3, BP4 and WPEN, are nonvolatile cells that have the same properties and functions as the regular memory cells.

Table 4-5. Sector/Block Write Protect Bits

Level	Status Register Bits				AT25FS010	
	BP4	BP3	BP1	BP0	Array Address	
locked Out	Locked-out Blocks					
0(none)	0	0	0	0	None	None
1(1/32)	0	1	0	0	01F000H – 01FFFFH	Sector 8 of Block 4
2(1/16)	1	0	0	0	01E000H – 01FFFFH	Sector 7 – 8 of Block 4
3(1/8)	1	1	0	0	01C000H – 01FFFFH	Sector 5 – 8 of Block 4
4(1/4)	x	x	0	1	018000H – 01FFFFH	ALL Sectors of Block 4
5(1/2)	x	x	1	0	010000H – 01FFFFH	ALL Sectors of Block 3,4
6(ALL)	x	x	1	1	000000H – 01FFFFH	ALL Sectors of ALL Blocks (1-4)

Note: 1. x = don't care

The WRSR instruction also allows the user to enable or disable the Write Protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is "1". Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is "0." When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the locked-out sectors in the memory array are disabled. Write is only allowed to sectors of the memory which are not locked out. The WRSR instruction is self-timed to automatically erase and program BP0, BP1, BP3, BP4 and WPEN bits. In order to write the status register, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then, $\overline{CS}$ must be low and the WRSR instruction and data for the six bits are entered. The WRSR write cycle will begin once $\overline{CS}$ goes high. During the internal write cycle, all instructions will be ignored except RDSR instructions. The AT25FS010 will automatically return to write disable state at the completion of the WRSR cycle. The status register is factory programmed to all 0's.

Note: When the WPEN bit is hardware write protected, it cannot be changed back to "0", as long as the $\overline{WP}$ pin is held low.

Table 4-6. WPEN Operation

WPEN	WP	WEN	ProtectedBlocks	UnprotectedBlocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

READ (READ): The READ instruction sequence reads the memory array up to the maximum speed of 50MHz. Reading the AT25FS010 via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the READ instruction is clocked in on the SI line, followed by the byte address to be read. Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line (see Figure 5-6). If only one byte is to be read, the $\overline{CS}$ line should be driven high after the least significant data bit. To continue read operation and sequentially read subsequent byte addresses from the device by simply keeping $\overline{CS}$ low and provide a clock signal. The device incorporates an internal address counter that automatically increments to the next byte address during sequential read operation. The READ instruction can be continued since the byte address is automatically incremented and data will continue to be shifted out of the AT25FS010 until the highest byte address is reached. When the last bit of the memory has been read, the device will continue reading back at the beginning of the array (000000h) without delay. The data is always output from the device with the most significant bit (MSB) of a byte first. The READ sequence is terminated any time $\overline{CS}$ is driven high and the device will go into standby mode.

FAST READ (FAST READ): The FAST READ instruction sequence reads the memory array up to the maximum speed of 50MHz (same as standard READ sequence). The FAST READ is an alternate command for the READ and allows for FAST READ instruction compatibility support. The difference between the two is FAST READ requires a “dummy byte” and READ does not. Reading the AT25FS010 via the SO (Serial Output) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the FAST READ instruction is clocked in on the SI line, followed by the byte address to be read and the dummy byte (the SO line output will be high Z state). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line (see Figure 5-7). If only one byte is to be read, the $\overline{CS}$ line should be driven high after the least significant data bit. To continue read operation and sequentially read subsequent byte addresses from the device by simply keeping $\overline{CS}$ low and provide a clock signal. The device incorporates an internal address counter that automatically increments to the next byte address during sequential read operation. The FAST READ instruction can be continued since the byte address is automatically incremented and data will continue to be shifted out of the AT25FS010 until the highest address is reached. When the last bit of the memory has been read, the device will continue reading back at the beginning of the array (000000h) without delay. The data is always output from the device with the most significant bit (MSB) of a byte first. The FAST READ sequence is terminated any time $\overline{CS}$ is driven high and the device will go into standby mode.

PROGRAM (PROGRAM): The PROGRAM instruction allows up to 256 data bytes to be written to each page in the memory in one-operation changing data bits from a logic 1 to 0 state. The AT25FS010 memory array contains 131,072 programmable data bytes internally organized into 256 bytes per page with a total of 512 pages in the memory.

In order to program the AT25FS010, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then the PROGRAM instruction can be executed and requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the PROGRAM instruction is clocked in via the SI line followed by the byte address (see Figure 5-8) and the data byte(s) to be programmed. Programming will start after $\overline{CS}$ pin is brought high. Please note: The low to high transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit to initiate programming cycle. Also, a WREN instruction must precede each and every PROGRAM instruction. The Ready/Busy status of the device can be determined by initiating a RDSR instruction. If bit 0=1, the program cycle is

still in progress. If Bit 0=0, the programming cycle has ended. Only the RDSR instruction is enabled during the programming cycle and all other opcode instructions are ignored until programming cycle has completed.

A single PROGRAM instruction programs 1 to 256 consecutive bytes within a page if it is not write protected. The starting byte address can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed is less than a full page, the data of all other bytes on the same page will remain unchanged meaning that the unwritten address locations within the page will not be changed. If more than 256 bytes of data are provided, the address counter will roll over on the same page and the previous data provided will be replaced. The same byte cannot be reprogrammed without erasing the whole sector or block first. The AT25FS010 will automatically return to the write disable state at the completion of the programming cycle.

Note: If the device is not write enabled (WREN), the device will ignore the Write instruction and will return to the standby state when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to re-initiate the serial communication.

Table 4-7. Address Key

Address	AT25FS010
A_N	A_{15} - A_0
Don't Care Bits	A_{23} - A_{17}

ERASE OPERATION: The AT25FS010 memory array is internally organized into uniform 4K byte sectors or uniform 32K byte uniform blocks (see Table 4-8). Before data can be reprogrammed, the sector or block that contains the data must be erased first. In order to erase the AT25FS010, there are three flexible erase instructions that can be executed as follows: SECTOR ERASE, BLOCK ERASE and CHIP ERASE instructions. A SECTOR ERASE instruction allows erasing any individual 4K sector without changing data in rest of memory. The BLOCK ERASE instruction allows erasing any individual block and CHIP ERASE allows erasing the entire memory array.

SECTOR ERASE (SECTOR ERASE): The SECTOR ERASE instruction sets all 4K bytes in the selected sector to logic 1 or erased state. In order to sector erase the AT25FS010, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then the SECTOR ERASE instruction can be executed and will erase every byte in the selected sector if the sector is not locked out. The sector address is automatically determined if any address within the sector is selected (see Figure 5-10). The SECTOR ERASE instruction is internally controlled and self timed to completion. During this time, all commands will be ignored except RDSR instruction. The progress or completion of the erase operation can be determined by reading ready/busy bit (bit 0) through RDSR instruction. If Bit 0=1, sector erase cycle is in progress. If Bit 0=0, the erase operation has been completed. The AT25FS010 will automatically return to the write disable state at the completion of the SECTOR ERASE cycle.

Table 4-8. Sector and Block Address

Block 4 1/4	1/8	1/16	1/32	Sector 8		01FFFFH
						01F000H
				Sector 7		01EFFFH
						01E000H
				Sector 6		01DFFFH
						01D000H
				Sector 5		01CFFFH
						01C000H
				Sector 4		01BFFFH
						01B000H
				Sector 3		01AFFFH
						01A000H
				Sector 2		019FFFH
						019000H
				Sector 1		018FFFH
						018000H
Block 3						017FFFH
						010000H
Block 2						00FFFFH
						008000H
Block 1						007FFFH
						000000H

BLOCK ERASE (BLOCK ERASE): The BLOCK ERASE instruction sets all 32K bytes in the selected block to logic 1 or erased state. In order to block erase the AT25FS010, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then the BLOCK ERASE instruction can be executed and will erase every byte in the selected block if the block is not locked out. The block address is automatically determined if any address within the block is selected (see Figure 5-11). The BLOCK ERASE instruction is internally controlled and self timed to completion. During this time, all commands will be ignored except RDSR instruction. The progress or completion of the erase operation can be determined by reading ready/busy bit (bit 0) through RDSR instruction. If Bit 0=1, block erase cycle is in progress. If Bit0=0, the erase operation has been completed. The AT25FS010 will automatically return to the write disable state at the completion of the BLOCK ERASE cycle.

CHIP ERASE (CHIP ERASE): As an alternative to the SECTOR ERASE/BLOCK ERASE, the CHIP ERASE instruction will erase every byte in all sectors that are not locked out. First, the device must be write enabled via the WREN instruction. Then the CHIP ERASE instruction can be executed. The CHIP ERASE instruction is internally controlled; it will automatically be timed to completion. The CHIP ERASE cycle time typically is 8 seconds. During the internal erase

cycle, all instructions will be ignored except RDSR. The AT25FS010 will automatically return to the write disable state at the completion of the CHIP ERASE cycle.

5. Timing Diagrams (for SPI Mode 0 (0, 0))

Figure 5-1. Synchronous Data Timing

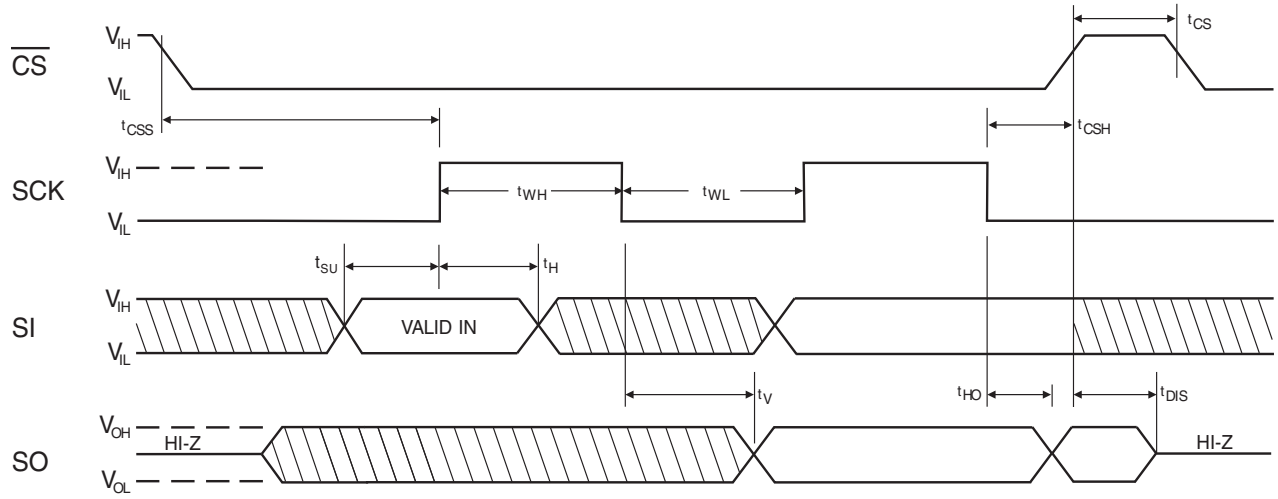


Figure 5-2. WREN Timing

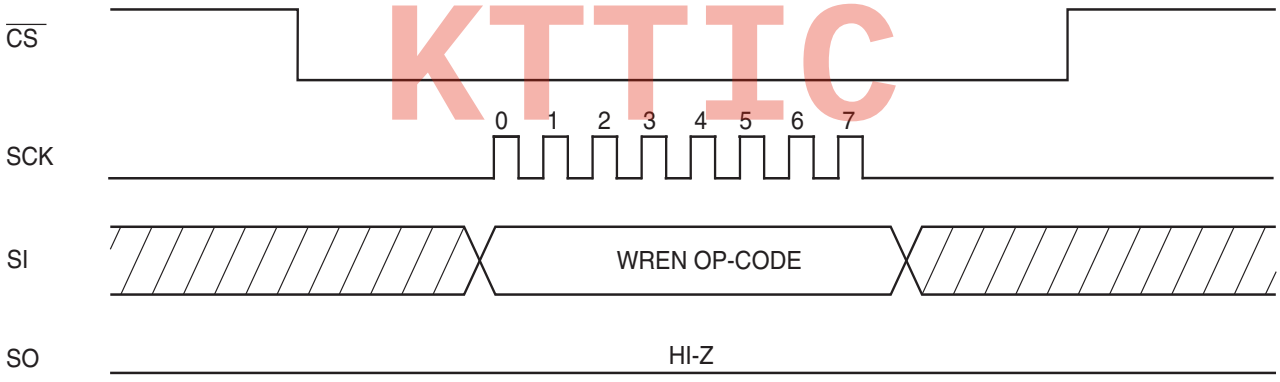


Figure 5-3. WRDI Timing

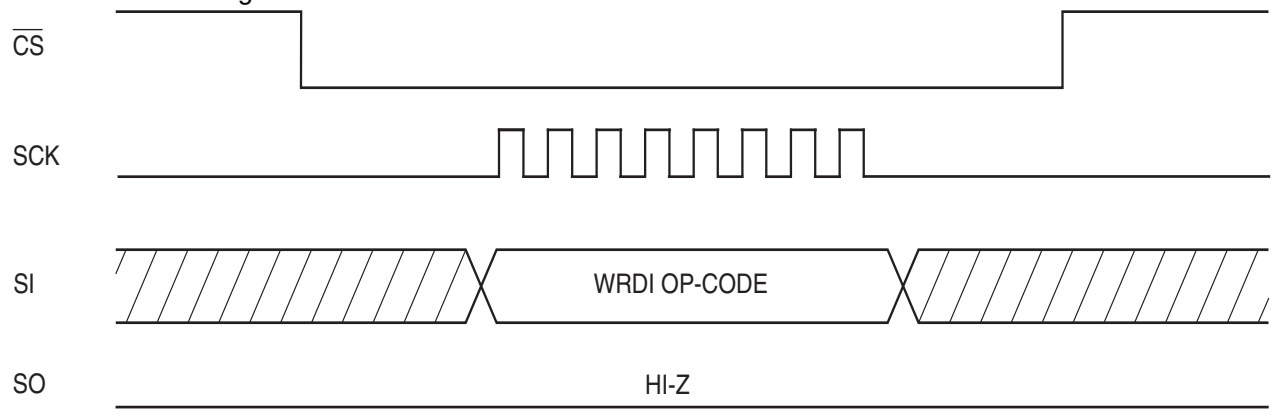


Figure 5-4. RDSR Timing

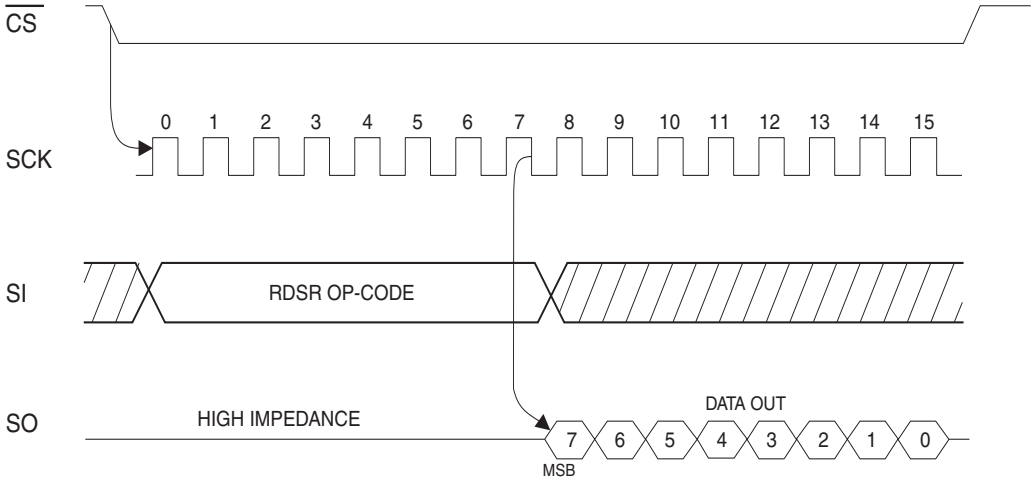


Figure 5-5. WRSR Timing

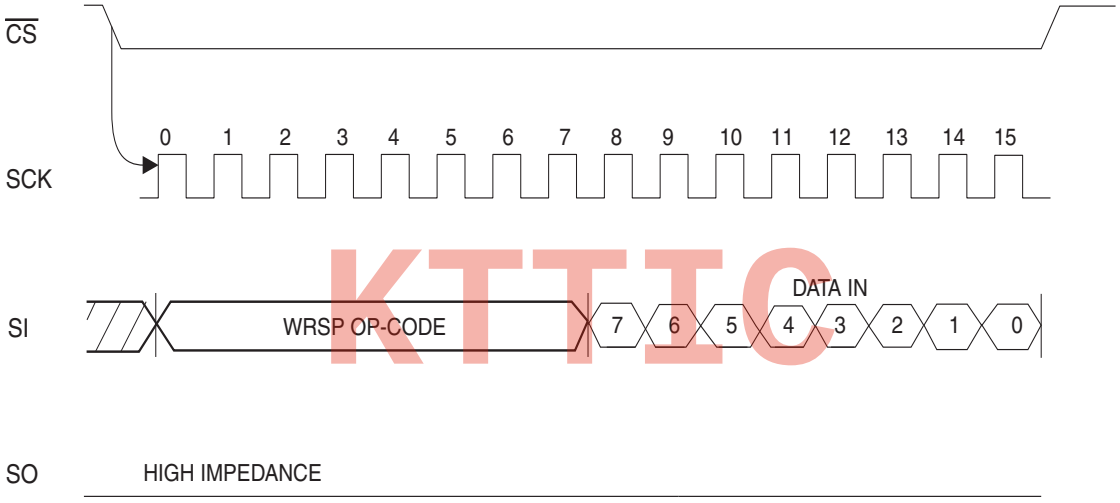


Figure 5-6. READ Timing

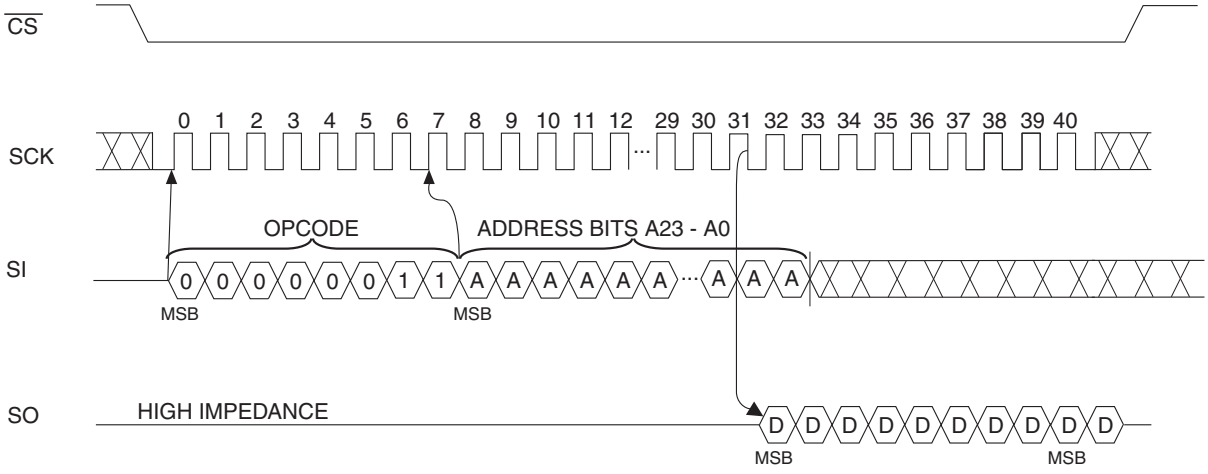


Figure 5-7. FAST READ Timing

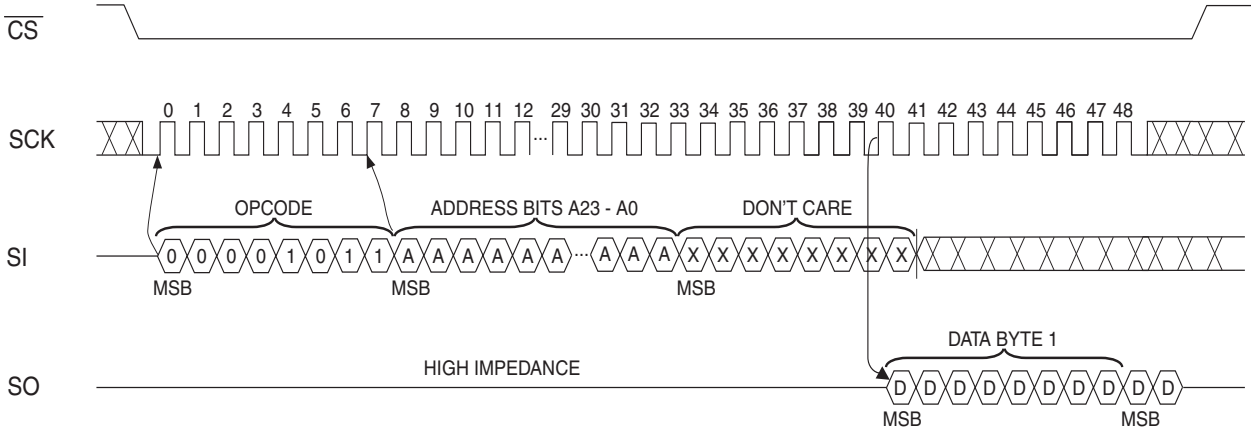


Figure 5-8. PROGRAM Timing

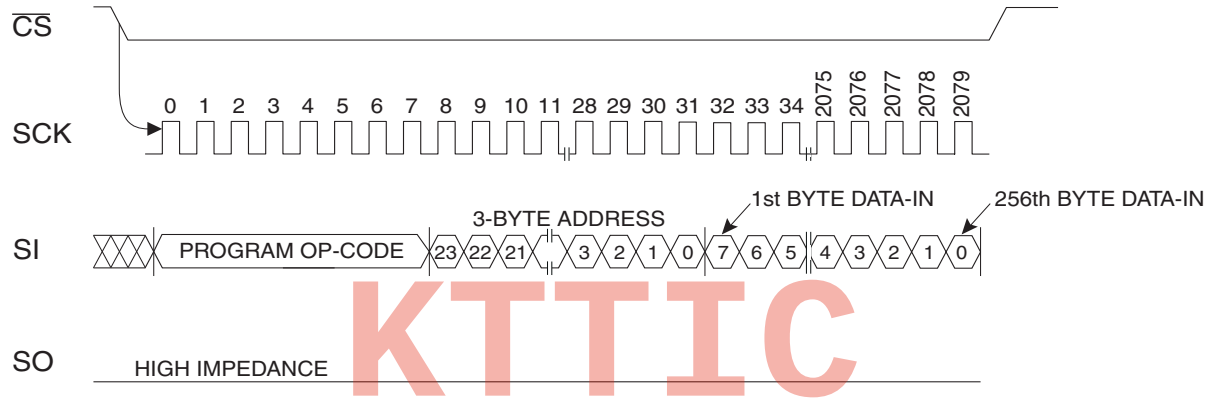


Figure 5-9. HOLD Timing

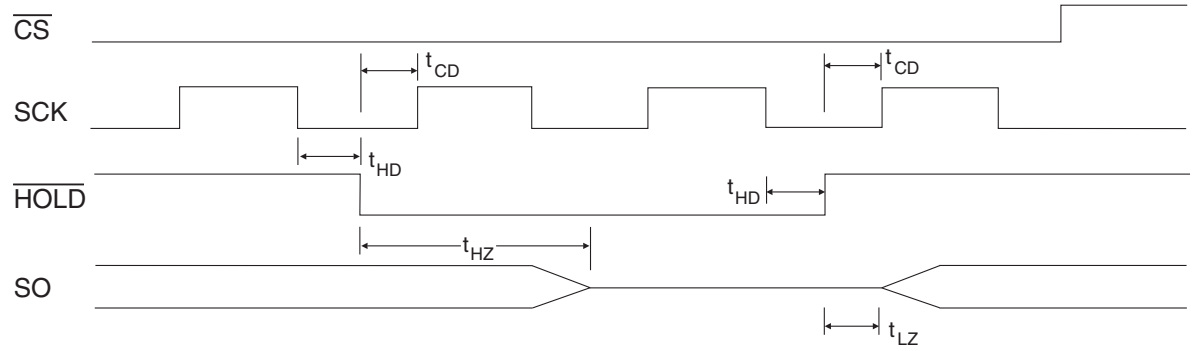


Figure 5-10. SECTOR ERASE Timing

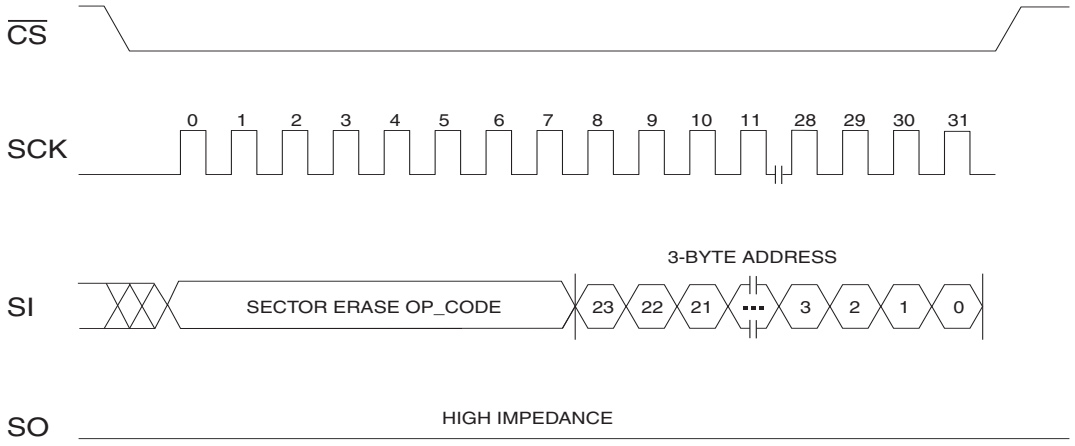


Figure 5-11. BLOCK ERASE Timing

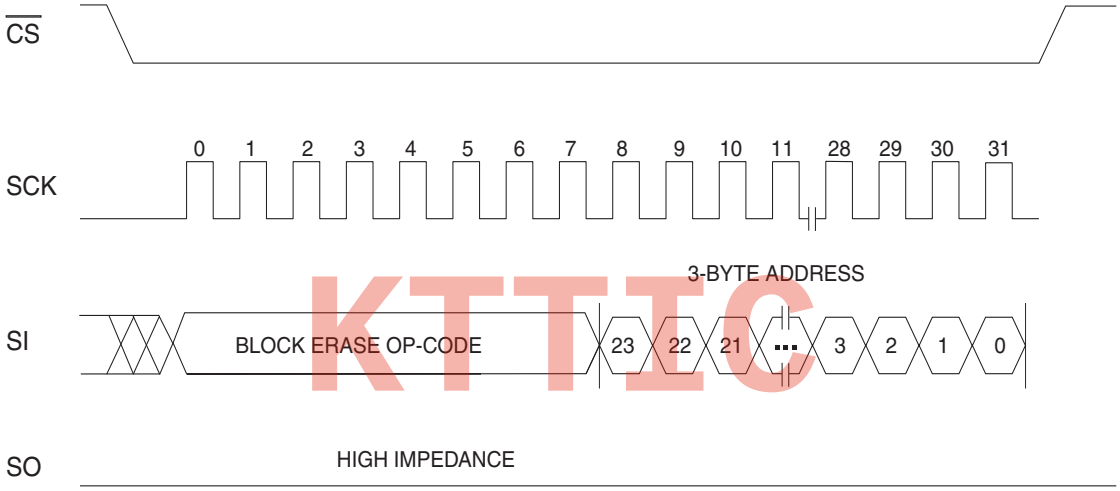


Figure 5-12. CHIP ERASE Timing

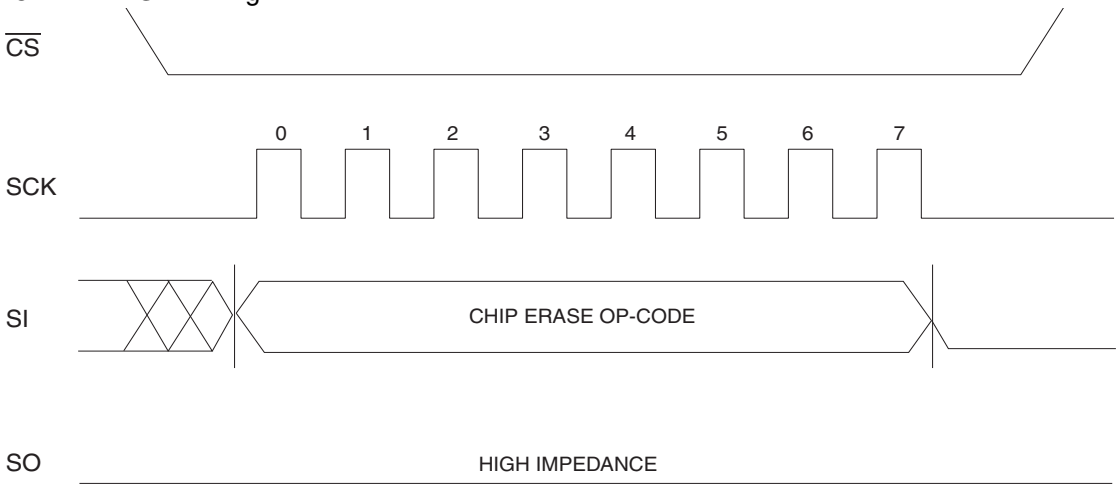
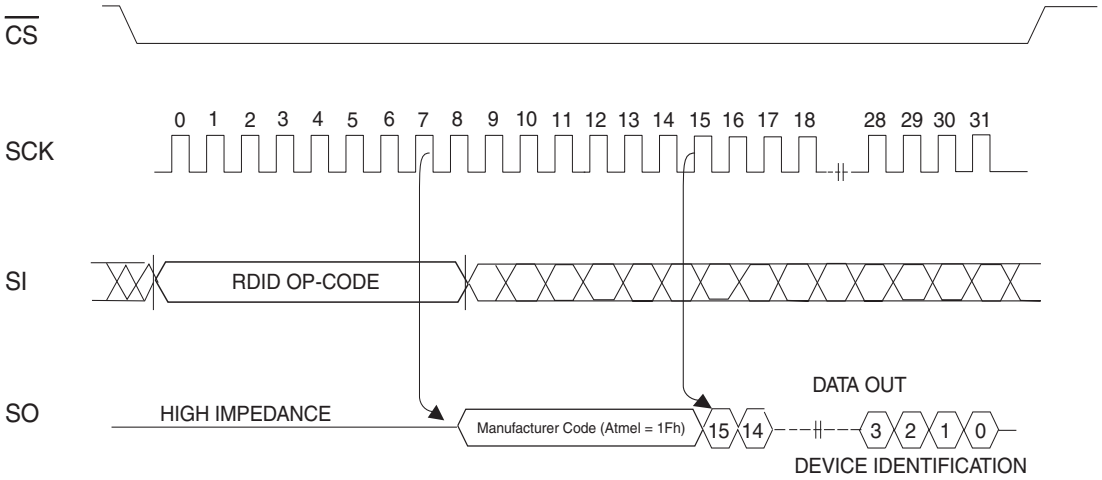


Figure 5-13. RDID Timing



Ordering Information

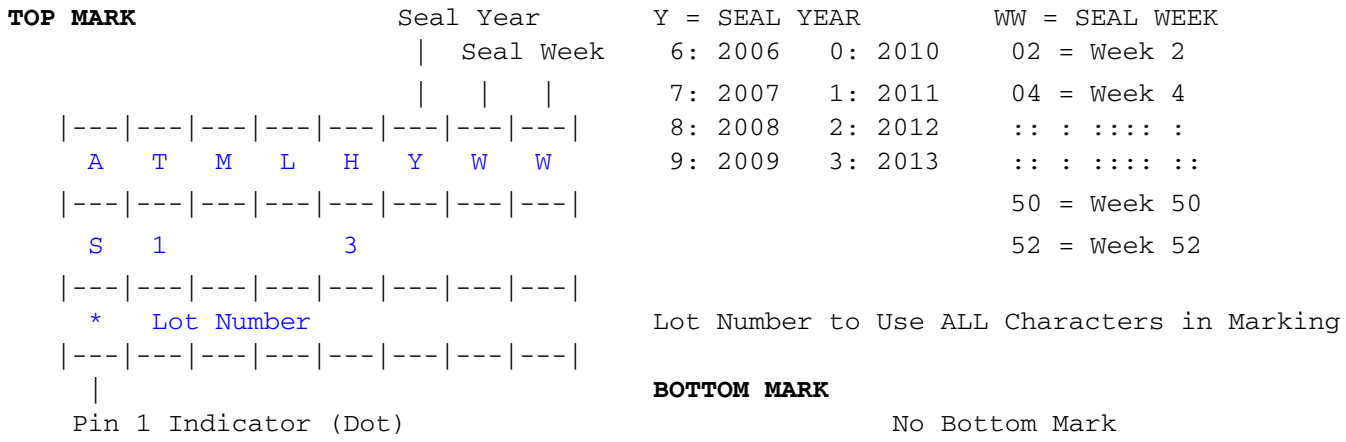
Ordering Code	Package	Operation Range
AT25FS010N-SH27-B[1]	8S1	Lead-Free/Halogen-Free/ NiPdAu Lead Finish Industrial Temperature (–40°C to 85°C)
AT25FS010N-SH27-T[2]	8S1	
AT25FS010Y7-YH27-T[2]	8Y7	

Notes: 1. "-B" designates bulk ordering code.
2. "-T" designates tape and reel ordering code. SOIC=4K per reel and SAP=3K per reel.

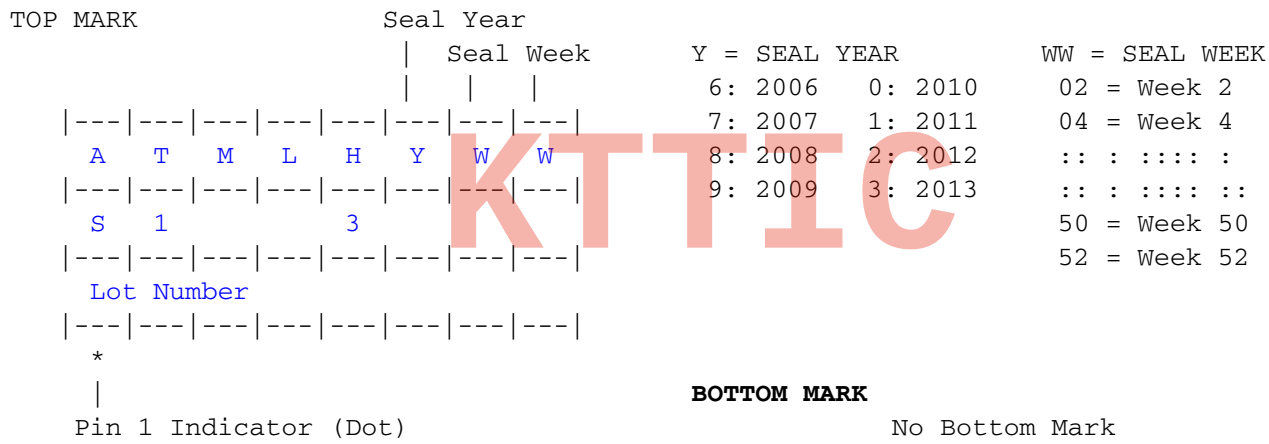
Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small outline (JEDEC SOIC)
8Y7	8-lead, 6.00 mm x 4.90 mm Body, Ultra Thin, Dual Footprint, Non-leaded, Small Array Package (SAP)
Options	
–2.7	Low Voltage (2.7V to 3.6V)

6. Part marking scheme

6.1 8-SOIC

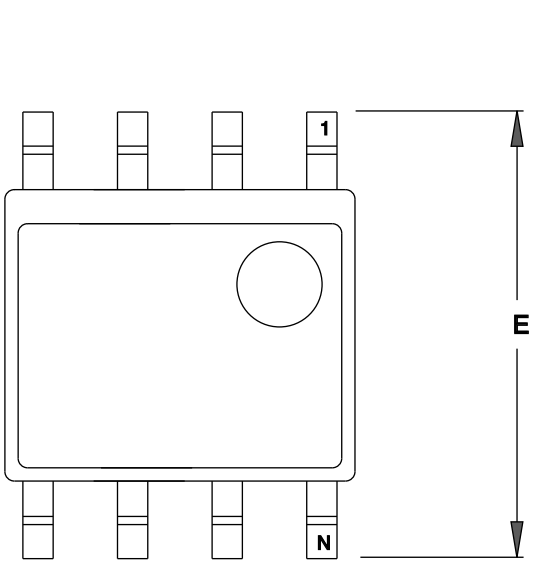


6.2 8-Ultra Thin SAP

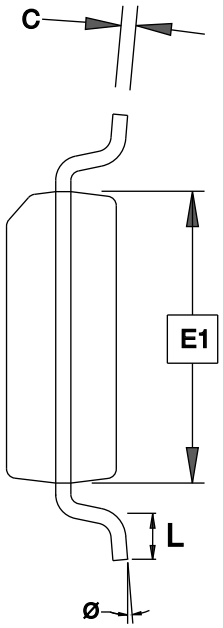


7. Package Information

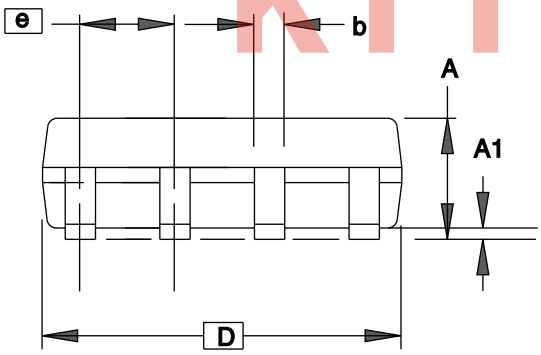
8S1 – JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

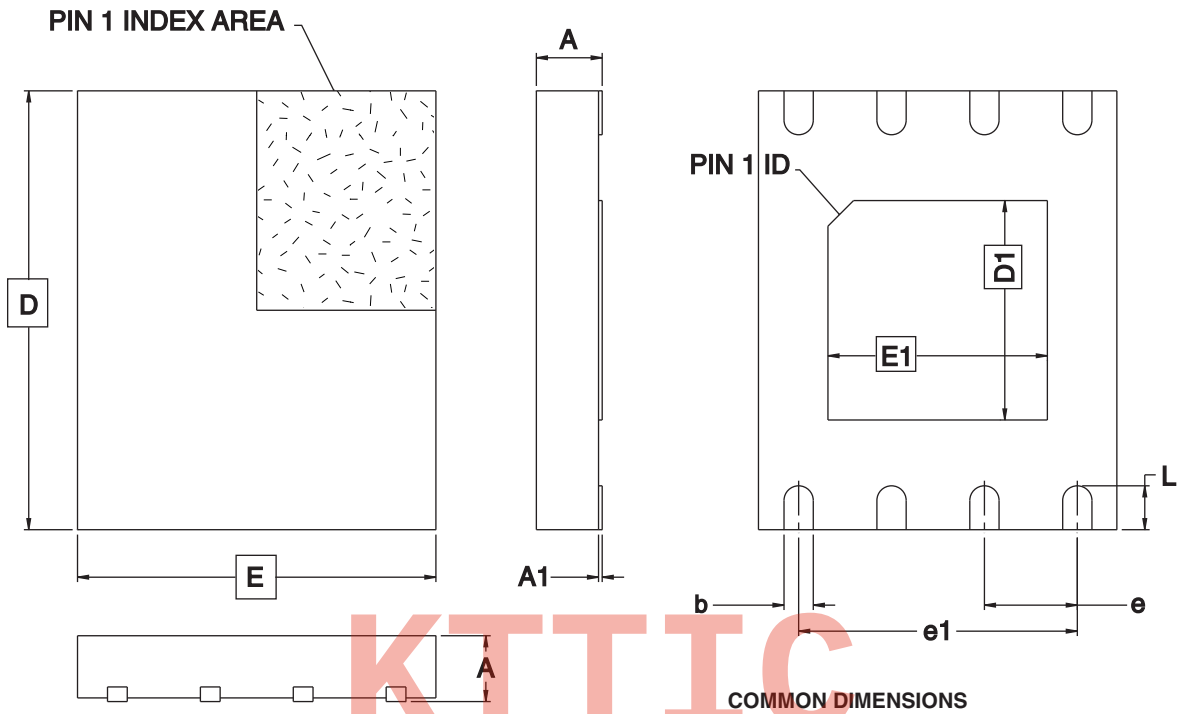
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
θ	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

3/17/05

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	8S1	C

8Y7 – SAP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.60	
A1	0.00	–	0.05	
D	5.80	6.00	6.20	
E	4.70	4.90	5.10	
D1	3.30	3.40	3.50	
E1	3.90	4.00	4.10	
b	0.35	0.40	0.45	
e		1.27 TYP		
e1		3.81 REF		
L	0.50	0.60	0.70	

10/13/05

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8Y7**, 8-lead (6.00 x 4.90 mm Body) Ultra-Thin SOIC Array Package (UTSAP) Y7	8Y7	B

8. Revision History

Doc. Rev.	Date	Comments
5167D	8/2007	Added Die Sales Info to Features Added lines to Ordering Codes table Updated to new Template Added Part Marking tables
5167C	4/2007	Changed 'Advance Information' to Preliminary
5167B	1/2007	Changed 'BLOCK ERASE(1)' operation from 64kbyte to 32kbyte on page 7.
5167A	8/2006	Initial document release.