## Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
  - Data Sheet Describes Mode 0 Operation
- Medium-voltage and Standard-voltage Operation
  - 2.7 ($V_{CC}$ = 2.7V to 5.5V)
- Extended Temperature Range –40°C to +125°C
- 5.0 MHz Clock Rate
- 8-byte Page Mode
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: One Million Write Cycles
  - Data Retention: 100 Years
- 8-lead JEDEC SOIC and 8-lead TSSOP Packages

## Description

The AT25010A/020A/040A provides 1024/2048/4096 bits of serial electrically-erasable programmable read-only memory (EEPROM) organized as 128/256/512 words of 8 bits each. The device is optimized for use in many automotive applications where low-power and low-voltage operation are essential. The AT25010A/020A/040A is available in space-saving 8-lead JEDEC SOIC and 8-lead TSSOP packages.

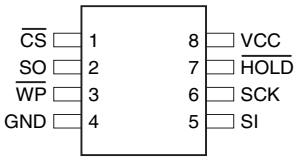
The AT25010A/020A/040A is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate erase cycle is required before write.

Block write protection is enabled by programming the status register with one of four blocks of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

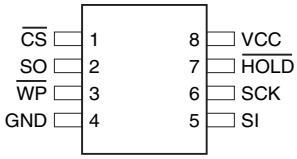
**Table 1.** Pin Configurations

| Pin Name | Function |
|---|---|
| $\overline{CS}$ | Chip Select |
| SCK | Serial Data Clock |
| SI | Serial Data Input |
| SO | Serial Data Output |
| GND | Ground |
| VCC | Power Supply |
| $\overline{WP}$ | Write Protect |
| $\overline{HOLD}$ | Suspends Serial Input |

8-lead SOIC




8-lead TSSOP




# SPI Automotive Temperature Serial EEPROMs

## 1K (128 x 8)
## 2K (256 x 8)
## 4K (512 x 8)

# AT25010A
# AT25020A
# AT25040A

5087D–SEEPR–3/07

## Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | –55°C to +125°C |
| Storage Temperature | –65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | –1.0V to +7.0V |
| Maximum Operating Voltage | 6.25V |
| DC Output Current | 5.0 mA |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 1.** Block Diagram

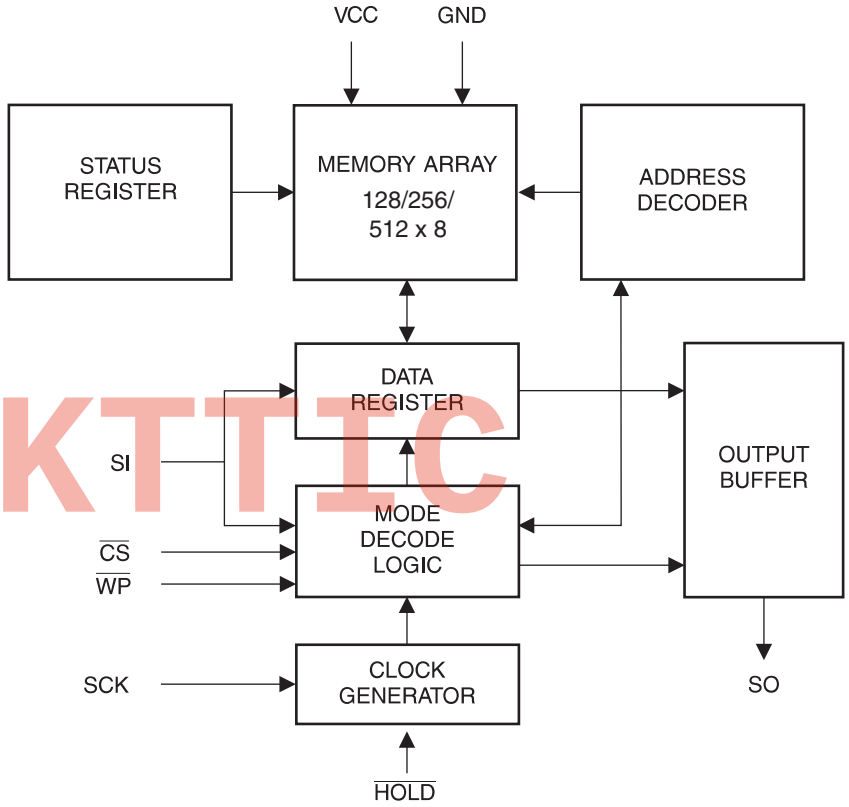


**Table 2.** Pin Capacitance[1]

Applicable over recommended operating range from $T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = +5.0V (unless otherwise noted)

| Symbol | Test Conditions | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance (SO) | 8 | pF | $V_{OUT}$ = 0V |
| $C_{IN}$ | Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$) | 6 | pF | $V_{IN}$ = 0V |

Note: 1. This parameter is characterized and is not 100% tested.

**Table 3.** DC Characteristics

Applicable over recommended operating range from: $T_A$ = –40°C to +125°C. $V_{CC}$ = +2.7V to +5.5V

| Symbol | Parameter | Test Condition | | Min | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC1}$ | Supply Voltage | | | 2.7 | 5.5 | V |
| $I_{CC1}$ | Supply Current | $V_{CC}$ = 5.0V at 1 MHz, SO = Open, Read | | | 3.0 | mA |
| $I_{CC2}$ | Supply Current | $V_{CC}$ = 5.0V at 2 MHz, SO = Open, Read, Write | | | 6.0 | mA |
| $I_{CC3}$ | Supply Current | $V_{CC}$ = 5.0V at 5 MHz, SO = Open, Read, Write | | | 6.0 | mA |
| $I_{SB1}$[1] | Standby Current | $V_{CC}$ = 2.7V | $\overline{CS}$ = $V_{CC}$ | | 3.0 | µA |
| $I_{SB2}$[1] | Standby Current | $V_{CC}$ = 5.0V | $\overline{CS}$ = $V_{CC}$ | | 5.0 | µA |
| $I_{IL}$ | Input Leakage | $V_{IN}$ = 0V to $V_{CC}$ | | –0.6 | 3.0 | µA |
| $I_{OL}$ | Output Leakage | $V_{IN}$ = 0V to $V_{CC}$ | | –0.6 | 3.0 | µA |
| $V_{IL}$[2] | Input Low Voltage | | | –0.6 | $V_{CC}$ x 0.3 | V |
| $V_{IH}$[2] | Input High Voltage | | | $V_{CC}$ x 0.7 | $V_{CC}$ + 0.5 | V |
| $V_{OL1}$ | Output Low Voltage | 3.6V ≤ $V_{CC}$ ≤ 5.5V | $I_{OL}$ = 2.0 mA | | 0.4 | V |
| $V_{OH1}$ | Output High Voltage | | $I_{OH}$ = –1.0 mA | $V_{CC}$ – 0.8 | | V |
| $V_{OL2}$ | Output Low Voltage | 2.7V ≤ $V_{CC}$ ≤ 3.6V | $I_{OL}$ = 0.15 mA | | 0.2 | V |
| $V_{OH2}$ | Output High Voltage | | $I_{OH}$ = –100 µA | $V_{CC}$ – 0.2 | | V |

Note: 1. Worst case measured at 125°C

2. $V_{IL}$ min and $V_{IH}$ max are reference only and are not tested.

**Table 4.** AC Characteristics

Applicable over recommended operating range from $T_A$ = –40°C to +125°C, $V_{CC}$ = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

| Symbol | Parameter | Voltage | Min | Max | Units |
|---|---|---|---|---|---|
| $f_{SCK}$ | SCK Clock Frequency | 2.7–5.5 | 0 | 5.0 | MHz |
| $t_{RI}$ | Input Rise Time | 2.7–5.5 | | 2 | µs |
| $t_{FI}$ | Input Fall Time | 2.7–5.5 | | 2 | µs |
| $t_{WH}$ | SCK High Time | 2.7–5.5 | 40 | | ns |
| $t_{WL}$ | SCK Low Time | 2.7–5.5 | 40 | | ns |
| $t_{CS}$ | $\overline{CS}$ High Time | 2.7–5.5 | 80 | | ns |
| $t_{CSS}$ | $\overline{CS}$ Setup Time | 2.7–5.5 | 80 | | ns |
| $t_{CSH}$ | $\overline{CS}$ Hold Time | 2.7–5.5 | 80 | | ns |
| $t_{SU}$ | Data In Setup Time | 2.7–5.5 | 5 | | ns |
| $t_H$ | Data In Hold Time | 2.7–5.5 | 20 | | ns |
| $t_{HD}$ | $\overline{Hold}$ Setup Time | 2.7–5.5 | 40 | | |
| $t_{CD}$ | $\overline{Hold}$ Hold Time | 2.7–5.5 | 40 | | ns |
| $t_V$ | Output Valid | 2.7–5.5 | 0 | 40 | ns |
| $t_{HO}$ | Output Hold Time | 2.7–5.5 | 0 | | ns |
| $t_{LZ}$ | $\overline{Hold}$ to Output Low Z | 2.7–5.5 | 0 | 40 | ns |
| $t_{HZ}$ | $\overline{Hold}$ to Output High Z | 2.7–5.5 | | 80 | ns |
| $t_{DIS}$ | Output Disable Time | 2.7–5.5 | | 80 | ns |
| $t_{WC}$ | Write Cycle Time | 2.7–5.5 | | 5 | ms |
| Endurance[1] | 5.0V, 25°C, Page Mode | | 1M | | Write Cycles |

Note: 1. This parameter is characterized and is not 100% tested.

## Serial Interface Description

**MASTER:** The device that generates the serial clock.

**SLAVE:** Because the serial clock pin (SCK) is always an input, the AT25010A/020A/040A always operates as a slave.

**TRANSMITTER/RECEIVER:** The AT25010A/020A/040A has separate pins designated for data transmission (SO) and reception (SI).

**MSB:** The Most Significant Bit (MSB) is the first bit transmitted and received.

**SERIAL OP-CODE:** After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed. The op-code also contains address bit A8 in both the Read and Write instructions.

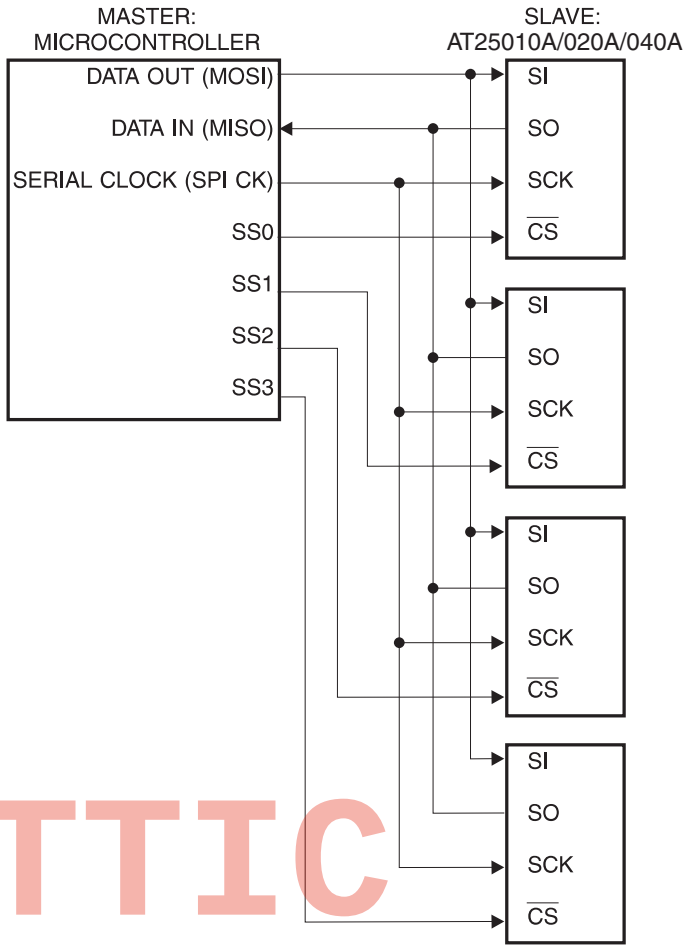
**INVALID OP-CODE:** If an invalid op-code is received, no data will be shifted into the AT25010A/020A/040A, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

**CHIP SELECT:** The AT25010A/020A/040A is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

**HOLD:** The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25010A/020A/040A. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

**WRITE PROTECT:** The write protect pin ($\overline{WP}$) will allow normal read/write operations when held high. When the WP pin is brought low, all write operations are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the AT25010A/020A/040A. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation.

**Figure 2.** SPI Serial Interface



## Functional Description

The AT25010A/020A/040A is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

The AT25010A/020A/040A utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 5. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low CS transition.

**Table 5.** Instruction Set for the AT25010A/020A/040A

| Instruction Name | Instruction Format | Operation |
|---|---|---|
| WREN | 0000 X110 | Set Write Enable Latch |
| WRDI | 0000 X100 | Reset Write Enable Latch |
| RDSR | 0000 X101 | Read Status Register |
| WRSR | 0000 X001 | Write Status Register |
| READ | 0000 A011 | Read Data from Memory Array |
| WRITE | 0000 A010 | Write Data to Memory Array |

Note: "A" represents MSB address bit A8.

**WRITE ENABLE (WREN):** The device will power up in the write disable state when $V_{CC}$ is applied. All programming instructions must therefore be preceded by a Write Enable instruction. The $\overline{WP}$ pin must be held high during a WREN instruction.

**WRITE DISABLE (WRDI):** To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

**READ STATUS REGISTER (RDSR):** The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the block write protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

**Table 6.** Status Register Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | BP1 | BP0 | WEN | $\overline{RDY}$ |

**Table 7.** Read Status Register Bit Definition

| Bit | Definition |
|---|---|
| Bit 0 ($\overline{RDY}$) | Bit 0 = "0" ($\overline{RDY}$) indicates the device is ready. Bit 0 = "1" indicates the write cycle is in progress. |
| Bit 1 (WEN) | Bit 1= "0" indicates the device is not write-enabled. Bit 1 = "1" indicates the device is write-enabled. |
| Bit 2 (BP0) | See Table 8 on page 8. |
| Bit 3 (BP1) | See Table 8 on page 8. |
| Bits 4 – 6 are "0"s when device is not in an internal write cycle. | |
| Bits 0 – 7 are "1"s during an internal write cycle. | |

**WRITE STATUS REGISTER (WRSR):** The WRSR instruction allows the user to select one of four levels of protection. The AT25010A/020A/040A is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any of

the data within any selected segment will therefore be read only. The block write protection levels and corresponding status register control bits are shown in Table 8.

Bits BP0 and BP1 are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, $t_{WC}$, RDSR).

**Table 8.** Block Write Protect Bits

| Level | Status Register Bits | | Array Addresses Protected | | |
|---|---|---|---|---|---|
| | BP1 | BP0 | AT25010A | AT25020A | AT25040A |
| 0 | 0 | 0 | None | None | None |
| 1 (1/4) | 0 | 1 | 60-7F | C0-FF | 180-1FF |
| 2 (1/2) | 1 | 0 | 40-7F | 80-FF | 100-1FF |
| 3 (All) | 1 | 1 | 00-7F | 00-FF | 000-1FF |

**READ SEQUENCE (READ):** Reading the AT25010A/020A/040A via the serial output (SO) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the read op-code (including A8) is transmitted via the SI line followed by the byte address to be read (A7–A0). Upon completion, any data on the SI line will be ignored. The data (D7–D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address, allowing the entire memory to be read in one continuous read cycle.

**WRITE SEQUENCE (WRITE):** In order to program the AT25010A/020A/040A, the Write Protect ($\overline{WP}$) pin must be held high and two separate instructions must be executed. First, the device *must be write enabled* via the WREN instruction. Then a write (WRITE) instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A write instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code (including A8) is transmitted via the SI line followed by the byte address (A7–A0) and the data (D7–D0) to be programmed. Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The READY/BUSY status of the device can be determined by initiating a read status register (RDSR) instruction. If Bit 0 = “1”, the write cycle is still in progress. If Bit 0 = “0”, the write cycle has ended. Only the RDSR instruction is enabled during the write programming cycle.

The AT25010A/020A/040A is capable of an 8-byte page write operation. After each byte of data is received, the three low-order address bits are internally incremented by one; the six high-order bits of the address will remain constant. If more than eight bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25010A/020A/040A is automatically returned to the write disable state at the completion of a write cycle.

**NOTE:** If the $\overline{WP}$ pin is brought low or if the device is not write enabled (WREN), the device will ignore the Write instruction and will return to the standby state when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to reinitiate the serial communication.

## Timing Diagrams

**Figure 3.** Synchronous Data Timing (for Mode 0)

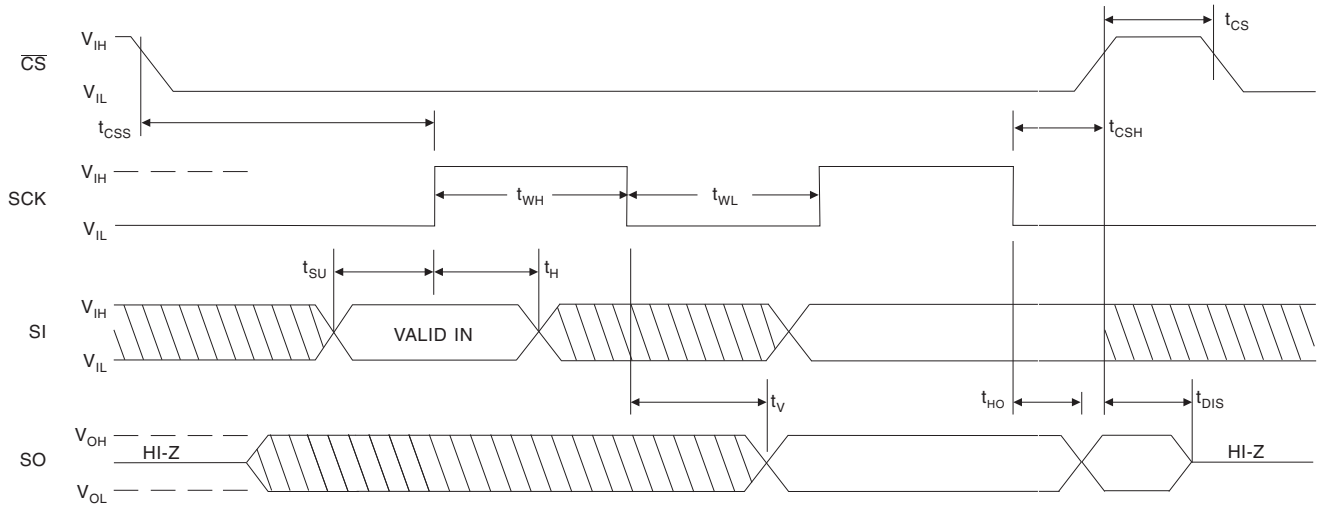



**Figure 4.** WREN Timing

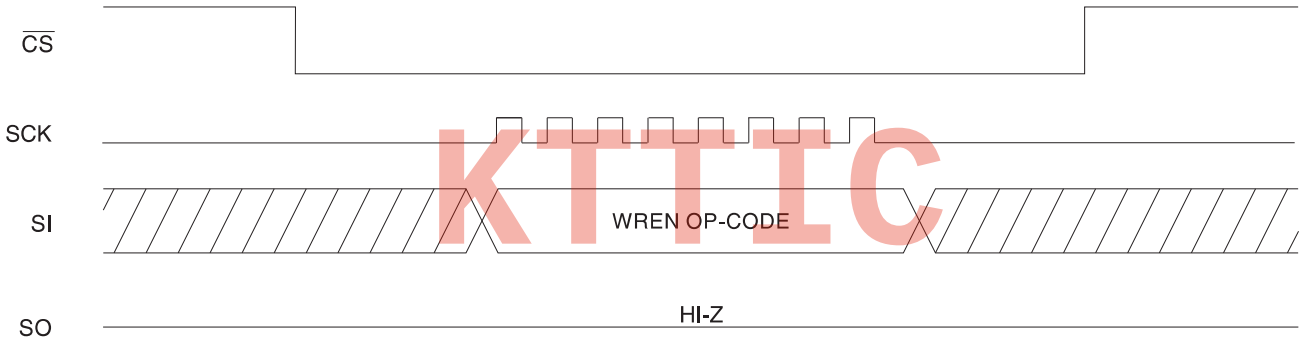



**Figure 5.** WRDI Timing

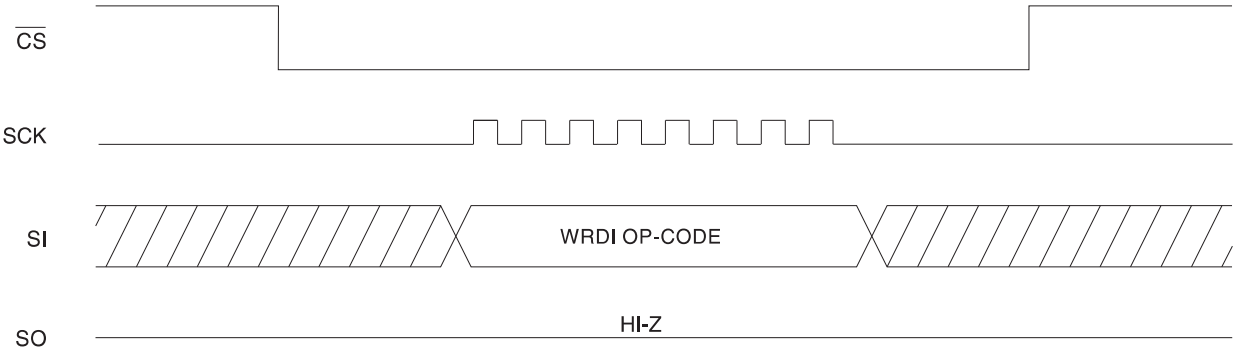


**Figure 6.** RDSR Timing

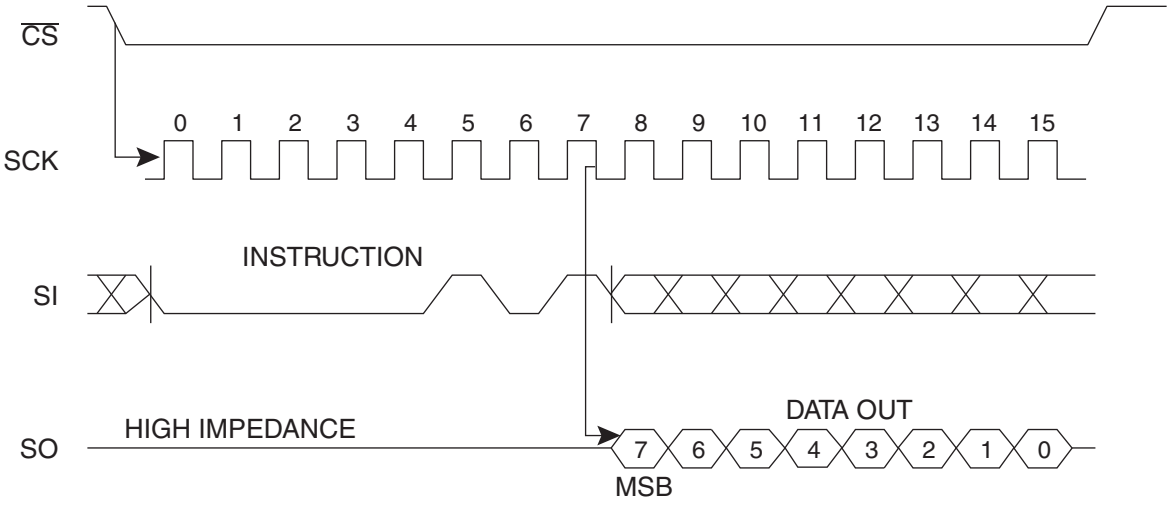



**Figure 7.** WRSR Timing

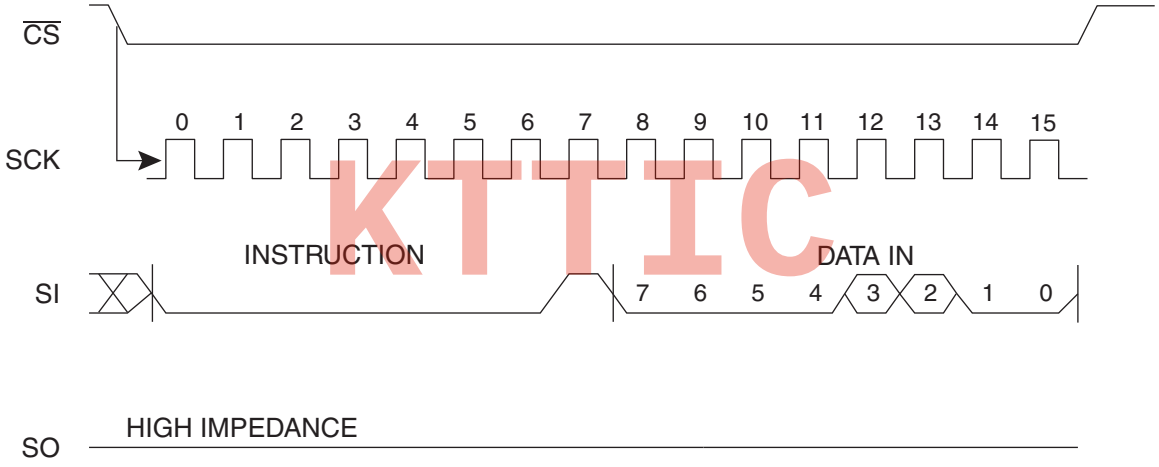


**Figure 8.** READ Timing

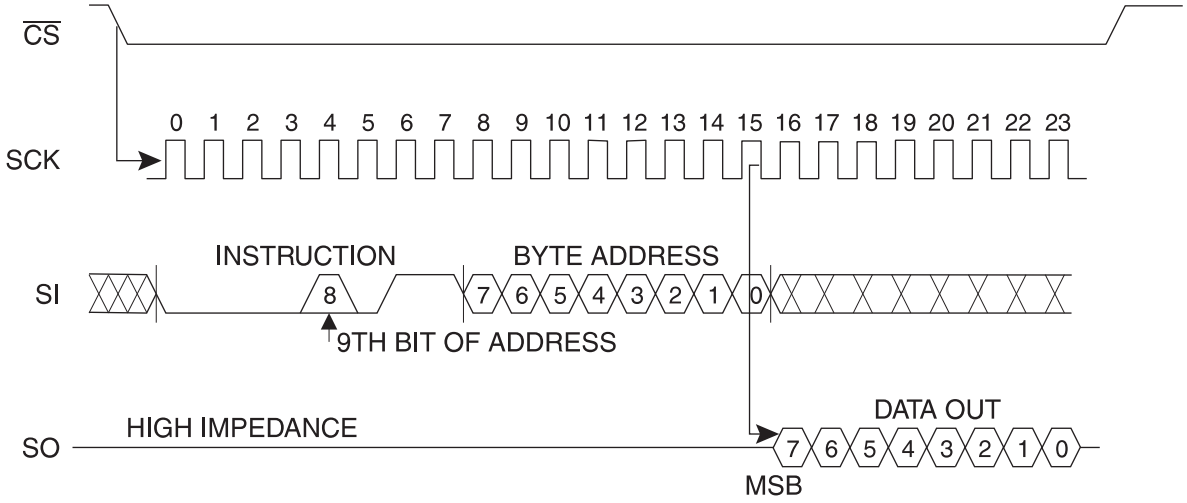



**Figure 9.** WRITE Timing

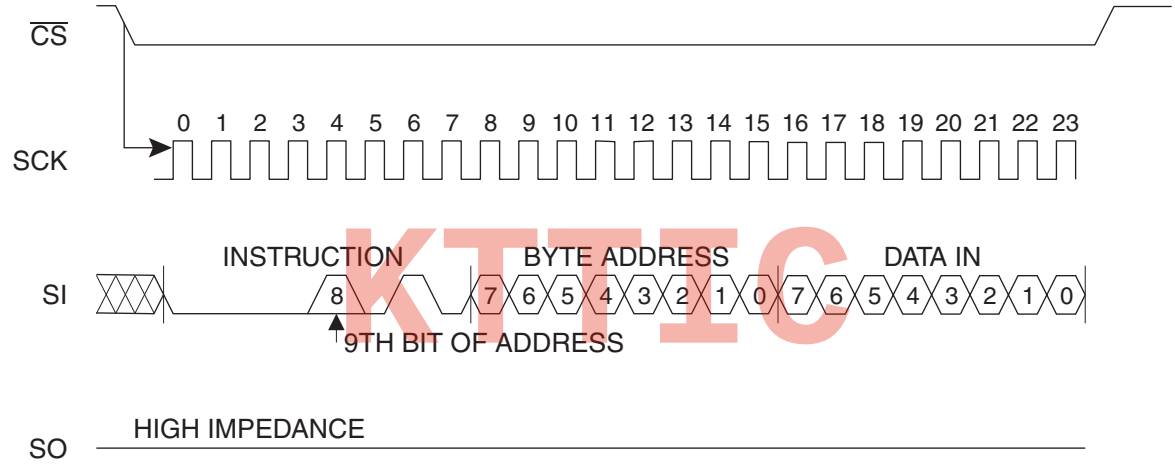
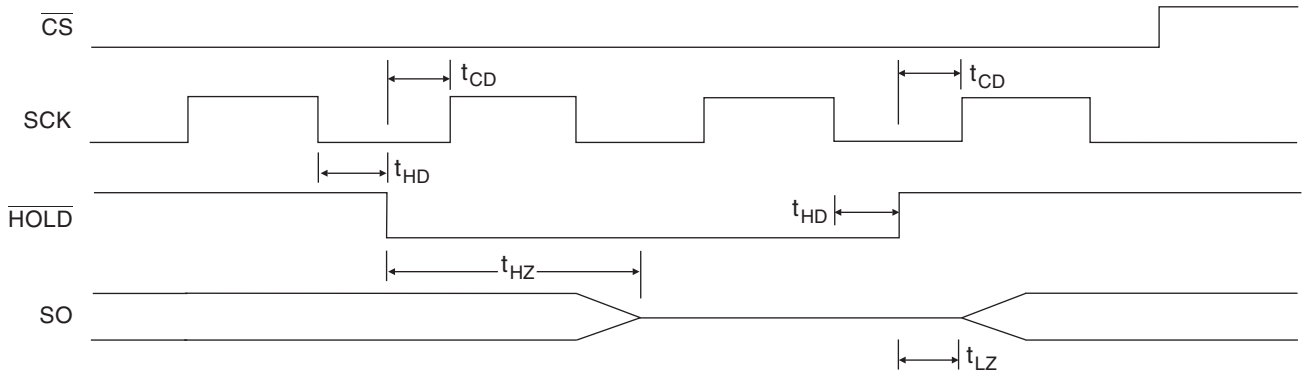



**Figure 10.** $\overline{HOLD}$ Timing



## AT25010A Ordering Information

| Ordering Code | Package | Operation Range |
|---|---|---|
| AT25010AN-10SQ-2.7<br>AT25010A-10TQ-2.7 | 8S1<br>8A2 | Lead-free/Halogen-free<br>Automotive Temperature<br>(–40°C to 125°C) |



| Package Type | |
|---|---|
| **8S1** | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| **8A2** | 8-lead, 0.170” Wide, Thin Shrink Small Outline Package (TSSOP) |
| **Options** | |
| **–2.7** | Low Voltage (2.7V to 5.5V) |

## AT25020A Ordering Information

| Ordering Code | Package | Operation Range |
|---|---|---|
| AT25020AN-10SQ-2.7<br>AT25020A-10TQ-2.7 | 8S1<br>8A2 | Lead-free/Halogen-free<br>Automotive Temperature<br>(–40°C to 125°C) |



| Package Type | |
|---|---|
| **8S1** | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| **8A2** | 8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP) |
| **Options** | |
| **–2.7** | Low Voltage (2.7V to 5.5V) |

## AT25040A Ordering Information

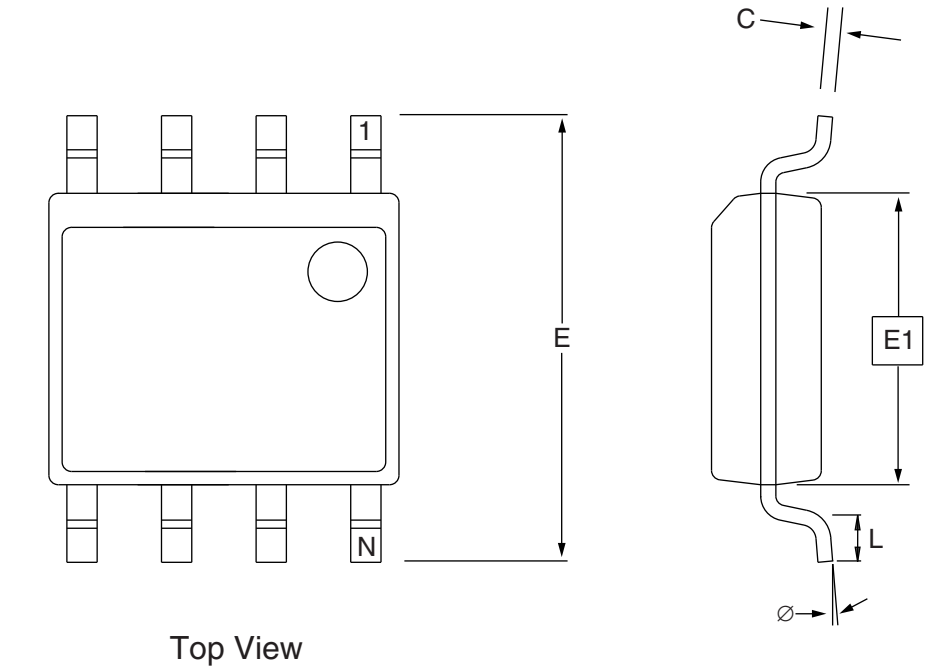
| Ordering Code | Package | Operation Range |
|---|---|---|
| AT25040AN-10SQ-2.7<br>AT25040A-10TQ-2.7 | 8S1<br>8A2 | Lead-free/Halogen-free<br>Automotive Temperature<br>(–40°C to 125°C) |

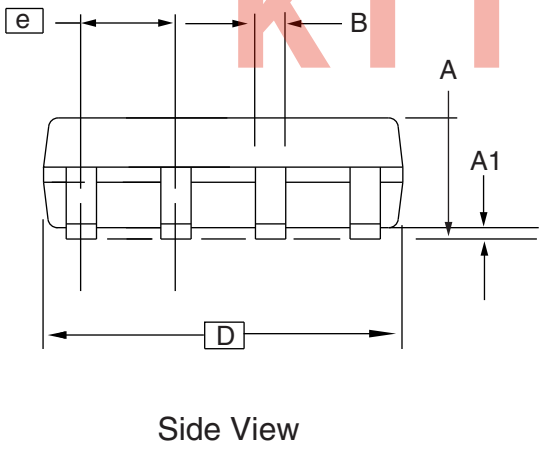


| Package Type | |
|---|---|
| **8S1** | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| **8A2** | 8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP) |
| **Options** | |
| **–2.7** | Low Voltage (2.7V to 5.5V) |

## Packaging Information

### 8S1 – JEDEC SOIC






**COMMON DIMENSIONS**
(Unit of Measure = mm)

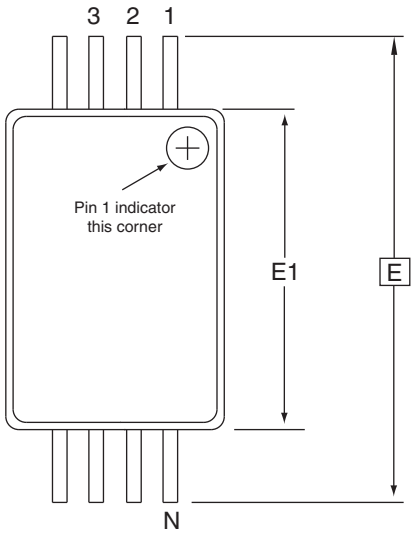
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 1.35 | – | 1.75 | |
| A1 | 0.10 | – | 0.25 | |
| b | 0.31 | – | 0.51 | |
| C | 0.17 | – | 0.25 | |
| D | 4.80 | – | 5.00 | |
| E1 | 3.81 | – | 3.99 | |
| E | 5.79 | – | 6.20 | |
| e | 1.27 BSC | | | |
| L | 0.40 | – | 1.27 | |
| ∅ | 0° | – | 8° | |

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

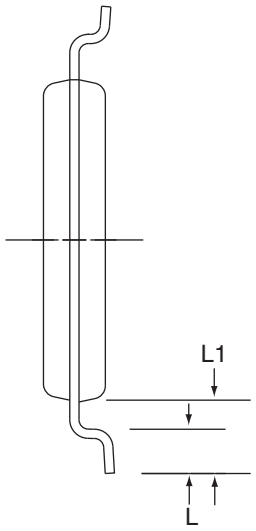
10/7/03

| | | | |
|---|---|---|---|
| 1150 E. Cheyenne Mtn. Blvd.<br>Colorado Springs, CO 80906 | **TITLE**<br>**8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC) | **DRAWING NO.**<br>8S1 | **REV.**<br>B |

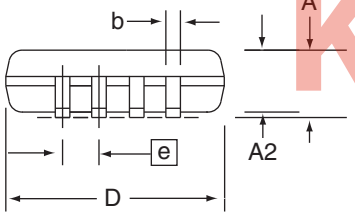
## 8A2 – TSSOP




Top View




End View




Side View

**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| D | 2.90 | 3.00 | 3.10 | 2, 5 |
| E | | 6.40 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 | 3, 5 |
| A | – | – | 1.20 | |
| A2 | 0.80 | 1.00 | 1.05 | |
| b | 0.19 | – | 0.30 | 4 |
| e | | 0.65 BSC | | |
| L | 0.45 | 0.60 | 0.75 | |
| L1 | | 1.00 REF | | |

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **8A2**, 8-lead, 4.4 mm Body, Plastic<br>Thin Shrink Small Outline Package (TSSOP) | 8A2 | B |

## Revision History

| Doc. Rev. | Date | Comments |
|---|---|---|
| 5087D | 3/2007 | Corrected package codes on pages 12 and 13 |
| 5087C | 2/2007 | Implemented revision history<br>Removed PDIP package offering<br>Removed PB'd parts |